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# Welcome Address

Welcome to the 25th Workshop On Compound Semiconductor Devices and Integrated Circuits held in Europe (Wocsdice 2001).

If you like evocative suggestions, there is something fascinating in considering this journey of our meeting: from Greece to Italy across the Mediterranean Sea: a (comfortable) Odyssey that, in 2001, brings the most advanced technological knowledge towards unexplored frontiers...
Arthur Clarke apart, there is in my opinion a very good point in having chosen Sardinia, Italy, as the place for WOCSDICE 2001. It belongs to Italy, of course, but it is a particular Italy, far from the leading edges of technology, and rich of history and nature; geographically far from the other lands, but shining with his own splendour and proud to be "singular". And singular events took place in Sardinia even in the Information Technology world: here the net was first used to break the insularity. The first newspaper on-line in the world was born here, many years ago. Now, it is from Sardinia that new stars of the Communication Market arose.
Few people (less than 2 millions), and two universities, at Sassari in the northern side, and Cagliari, the main town of the island, where the very recent birth of the course of Electron Engineering first brought the language of microelectronic physics and technology. Many of us, professors, came from other towns, with the duty to start up this new adventure. Many links with old friends, cooperation with more celebrated universities and a lot of daily work were the ingredients to play with.
And now such a top event as WOCSDICE honours our efforts.
Let me then tray to pay, in this page, part of the huge debts that I got with the many people who helped me. I wish to thank the Office of Naval Research International Field Office (ONR-IFO) and the U.S. Army Research Laboratory - European Research Office (ARL-ER) for their financial support.
For the same reason I will thank the Organisations to which I belong, the University of Cagliari and the National Institute for Solid State Physics (Istituto Nazionale di Fisica della Materia, INFM).
Thanks also to the logistic contribution from the many local administration offices: the Assessorato al Turismo and the Azienda Autonoma di Soggiorno e Turismo of the town of Cagliari, the corresponding Ufficio del Turismo of Quartu S.Elena, the Ente Provinciale del Turismo (EPT) and the Ente Sardo Industrie Turistiche (ESIT).

And very very special thanks to Cinzia and Rosalba and Gigi, of Informatic Service for their daily assistance during the past months up to now for creating the event.

Last, let me indicate the real chairman of WOCSDICE 2001, who solicited, selected, distributed, invited peoples and papers, my friend Gaudenzio Meneghesso, who will bring this appreciation to his University, the ancient and honourable University of Padua that, thanks to him, is the actual co-organizer of WOCSDICE 2001.
His job is simply and impressively summarized in the huge program that follows this welcome address.

Welcome again, a lot of thanks, too. And at the next appointment, WOCSDICE will have a new group of colleagues and friends: form here, Cagliari, Sardinia, Italy.

Massimo Vanzi
WOCDICE2001 Chair

# WOCSDICE 2001
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# INVITED SPEAKERS

**The low frequency noise in electronic devices: an engineering sight.**
*M. Borgarino and F. Fantini*
Dipartimento di Scienze dell'Ingegneria and INFM, Universita' di Modena e Reggio Emilia, via Vignolese 905, 41100 Modena, Italy

**Wide Bandgap Semiconductors Technologies for Microwave Power Amplifiers.**
*C. Brylinski*
THALES LCR (formerly Thomson-CSF/LCR) Domaine de Corbeville, F-91404 Orsay Cedex

**GaInP-GaAs HBT's for High Frequency and High Power Applications.**
*S.L. Delage, D. Floriot, S. Cassette, N. Caillas, E. Chartier, N. Frapsauce, M. Surrugue, J.C. Jacquet, S. Piotrowicz, M.A.diForte-Poisson*
THALES LCR (formerly Thomson-CSF/LCR) Domaine de Corbeville, F-91404 Orsay Cedex

**Development of InGaN on SiC LED and lasers at OSRAM.**
*V. Härle*
Osram Opto Semiconductors GmbH & Co. OHG

**PBG-like frequency and angular selective devices.**
*J. Danglot, T. Akalin, O. Vanbésien and D. Lippens*
Institut d'Electronique et de Microélectronique du Nord - Université des Sciences et Technologies de Lille -59652 Villeneuve d'Ascq Cedex, France

**GaN on Silicon for High Power and High Frequency Electronics.**
*E. L. Piner*
Nitronex Corporation, 628 Hutton Street, Suite 103 Raleigh, NC 27606.

**AlGaN/GaN HEMT's: epitaxial growth issues on various substrates, devices fabrication, and insertion of GaN component into circuits.**
*J. Smart*
V.P. of advanced Technology,RF Nitro Communications

**Design and Fabrication Technology of Gate and Gate Recess for Ultrahigh-Speed InP-Based HEMTs.**
*T. Suemitsu[a], T. Ishii[a] and H. Yokoyama[b]*
(a) NTT Photonics Laboratories 3-1 Morinosato Wakamiya, Atsugi, Kanagawa 243-0198, Japan
(b) NTT Advanced Technology Corp. 3-1 Morinosato Wakamiya, Atsugi, Kanagawa 243-0198, Japan

**New frontiers of Quantum Cascade devices: towards a THz laser.**
*A.Tredicucci[a], R. Köhler[a] R. Colombelli[b], F. Capasso[b], C. Gmachl[b], M. C. Wanke[b], A. L. Hutchinson[b], D. L. Sivco[b], and A. Y. Cho[b]*
(a)Scuola Normale Superiore and INFM, Piazza dei Cavalieri 7, I-56126 Pisa (Italy)
(b)Bell Laboratories, Lucent Technologies, 600 Mountain Avenue, Murray Hill, NJ 07974 (USA)

**Premature Saturation in AlGaN/GaN HFET's.**
*R.J. Trew*
ECE Department, Virginia Tech University, Blacksburg, VA

# SESSION I
# MMIC and Advanced Circuits
# Chair: Prof. Hans L. Hartnagel
# Monday May 28, 2001

| | |
|---|---|
| **8.40 am**<br><br>**INVITED** | **PBG-like frequency and angular selective devices**<br>*J. Danglot, T. Akalin, O. Vanbésien and D. Lippens*<br>Institut d'Electronique et de Microélectronique du Nord – Université des Sciences et Technologies de Lille -59652 Villeneuve d'Ascq Cedex, France |
| **9.05 am** | **Ultra Compact Reflective Type Phase Shifter MMIC for L-Band**<br>*F. Ellinger, R. Vogt and W. Bächtold,*<br>ETH-Zürich, CH-8092 Zürich, Switzerland, |
| **9.20 am** | **Monolithic Integration of Optoelectronic III/V Devices with Silicon-Microelectronics**<br>*D. Fehly, H.-H. Wehmann and A. Schlachetzki*<br>Institute for Semiconductor Technology Technical University Braunschweig, Braunschweig, Germany |
| **9.35 am** | **Monolithically Integrated Traveling-Wave Amplifier for Low-Cost Broadband Optical Receiver**<br>*A. Orzati and W. Bächtold*<br>Swiss Federal Institute of Technology, Gloriastrasse 35 CH-8092 Zurich, Switzerland |
| **9.50 am** | **III-V material and device aspects for the monolithic integration of GaAs devices on Si using GaAs/Si low temperature wafer bonding**<br>*A. Georgakilas[(a)], M. Alexe[(b)], G. Deligeorgis[(a)], D. Cengher[(a)], E. Aperathitis[(a)], Z. Hatzopoulos[(a)] and G. Halkias[(c)]*<br>(a) Microelectronics Research Group, FORTH, IESL and Univ. Crete, Physics Dept., P.O. Box 1527, 711 10, Heraklion-Crete, Greece<br>(b) Max Planck Institute of Microstructure Physics, Weinberg 2, D-06120 Halle, Germany<br>(c) NCSR "Demokritos", Inst. of Microelectronics, P.O. Box 60228, 15310 Agia Paraskevi, Greece |
| **10.05 am** | **Influence of the Integration on the Performance of Bidirectional Modules for Single Fiber Application**<br>*H.-C. Neitzert[(a)] and A. Piccirillo[(b)]*<br>(a) Università di Salerno, DIIIE, Fisciano, Italy,<br>(b) Telecom Italia Lab, Torino, Italy |

# PBG-like frequency and angular selective devices

J. Danglot, T. Akalin, O. Vanbésien and D. Lippens

Institut d'Electronique et de Microélectronique du Nord
Université des Sciences et Technologies de Lille
59652 Villeneuve d'Ascq Cedex, France

**Abstract** : The frequency and angular selectivity properties of PBG-like microstructures are more specially addressed with the aim to use them for innovative filtering and radiating elements. The concepts, used here, are quite general and can be applied to both optical and microwave devices. We exemplified the potential of such structures with three examples. Two concern the possibility of (i) fabricating compact filters with a two-side microstrip approach, the potential application being modules for steerable rf antenna and (ii) the micromachining of optical waveguides with the generic OADM multiplexer for WDM. The third one is dealing with the possibilities afforded by PBG structures for improving the radiation pattern of rf and optical sources.

**Introduction**:

Photonic Band gap (PBG's) Material systems are now attracting much interest with the prospect of high performance devices aimed at operating at microwave or optical frequencies [1]. Basically a periodic modulation of the refractive index (the permittivity) induces forbidden gaps in their electromagnetic spectrum. On the other hand, the modulation of their structure, in a fashion similar to the semiconductor potential, gives rise to an angular selectivity such as the anisotropy resulting from the crystallographic directions.
In this communication, we take advantage of such properties for analyzing filtering and radiating elements. To address these possibilities we report on (i) the microstrip-type filter with the structuring of their ground plane, (ii) a radiating element embedded in a Fabry-Pérot cavity and (iii) a directional coupler for the ADD DROP operation.

**Two side patterning for microstrip-type filters**

We report first on experimental analysis of photonic band gap microstrip-type filters by means of vectorial analysis at microwave frequencies. The periodically frequency selective structure was achieved via ground plane patterning and the influence of a shielding in close proximity was more specially addressed.

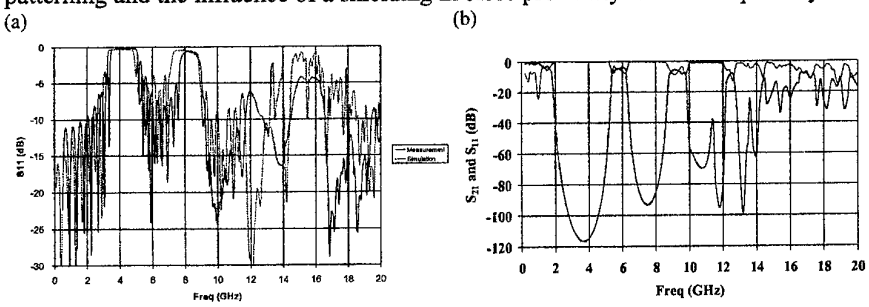


Fig. 1 frequency spectrum for the one side protoptype (a) and the two side circuit (b)

We used a relatively quite high dielectric constant for the microstrip substrate with a 1.27 mm-thick duroid 6010 (dielectric permittivity of 10). The prototypes were fabricated at the University of Pampelona by conventional printed-circuit techniques including the surface drilling of holes. Fig. 1 (a) and (b) shows the frequency dependence of the scattering parameters $S_{11}$ and $S_{21}$ measured and calculated using the HFSS code. A satisfactory agreement can be noted in the magnitude and the frequency of pass and stop band at least up to 10 GHz. The novelty in the present work stems from the combination of two patterns, one implemented upside as for a conventional microstrip filter with inductive and capacitive transmission line sections whereas the other one was patterned with holes. Figure 1(b) shows the calculated S11 and S21 scattering parameters for a two side structure filter. The top pattern is formed via a printed technology with successive high and low impedance section w1= 1.2mm and w2 = 8mm respectively. The back side ground plate is etched with holes of radius 3.5mm with a period of 14.1 mm. The holes are under the high impedance sections.

## Directive antenna [2]

In this section, we investigate the conditions of directivity for dipole antennas (Fig. 2(a)) embedded in PBG-like cavities. It is shown that the primary reason for a high directivity is the evanescence of electromagnetic wave in the PBG mirror. In practice, this implies to operate in the forbidden gap of the PBG material which constitutes the mirrors. A high transmission level of the structure, taken as a whole, is explained by a defect-assisted resonant transmission (2(b)). Under these conditions, simple Bragg reflectors 1D-photonic Band Gap structure can be used. This auto-focus effect (2(c)) is similar to that demonstrated over the past with resonant cavity antenna bounded by Bragg reflectors.

(a) (b) (c)

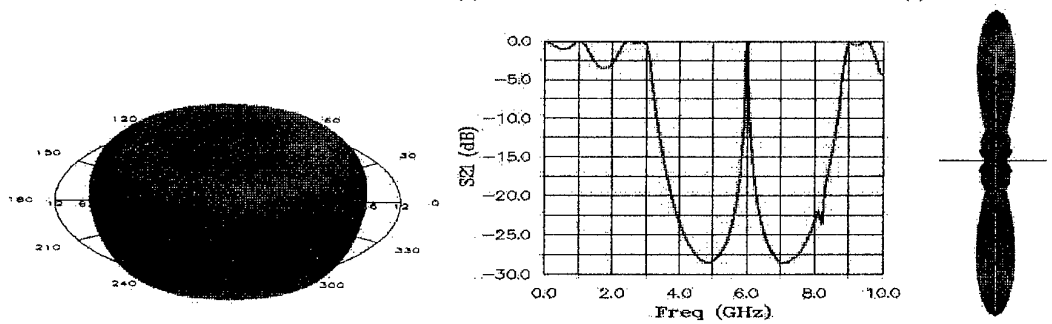


Figure 2 illustration of lens effect (a) radiation pattern for an isolated dipole (b) the resonant effect in the gap and (c) the focusing effect

## Optical Add Drop [3]

The conditions for frequency selective coupling between two electromagnetic waveguides in a Photonic Band Gap dielectric technology (Fig. 3(a)) are investigated using a whispery Gallery mode resonator. The study is conducted via electromagnetic simulations (3(b)) by addressing the directivity and selectivity issues. It is shown that the direction of feeding is essential in the directivity issue with interference patterning. As expected with a proper choice of PBG configuration, high intrinsic quality factor cavity can be demonstrated so that the loaded cavity meets the requirement of highly selective add or drop operation (3(c)). The possibility to preserve the coupling performances under finite vertical structuring is on the other hand addressed.

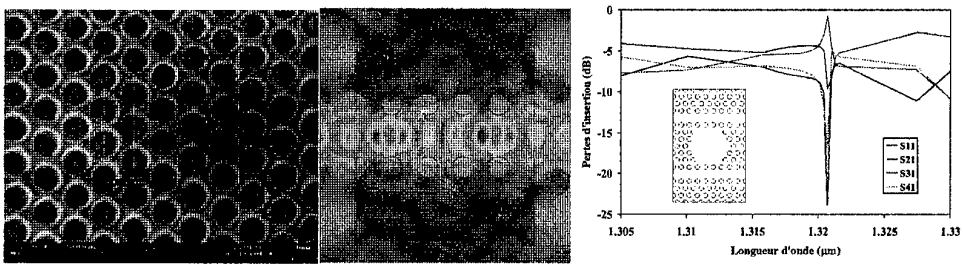


Figure 3 illustration of the PBG-like technology for integrated optics (a) hole drilling in a semicoductor on a submicron scale (b) modeling of the guiding propoerties with a linear defect (c) directional coupling.

## Conclusion.

Numerous degrees of freedom are now afforded by the use of PBG-like structure. In this context we demonstrated the concepts of wave guiding and filtering via distributed or local defects are quite general with potential applications in FDM and WDM.

Acknowledgement: The work on filter was carried out in the frame work of a collaboration with the Pampelona University. The study on integrated optics is supported by a french research agency contract.

## References

[1] See for instance Photonic Band Gap material edited by C.M. Soukoulis, Kluwer Academic Publishers

[3] T. Akalin et al. 24th ESTEC Antenna Workshop on innovative periodic antenna, photonic band gap, fractal and frequency selective structures , May/June 2001

[4] J. Danlot, et al. , IEEE Microwave and Guided Wave Letters, Vol. 9, N°7, July 1999

# Ultra Compact Reflective Type Phase Shifter MMIC for L-Band

Frank Ellinger, Rolf Vogt and Werner Bächtold,
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*Abstract* —**This paper presents an ultra compact reflective type MMIC phase shifter at 1.2 GHz for an aero navigation radar, which has been fabricated using a commercial GaAs MMIC process. A 3 dB 90° coupler with lumped elements was used to significantly reduce the circuit size in comparison to former approaches using microstrip branch-line or lange couplers. A phase shift range of 210° is obtained using reflective loads, which can be varied by MESFET varactors. The loss is 4.6 dB ± 1 dB, the 1 dB input compression point is higher than 7 dBm and the chip area is only 0.9 mm$^2$. To our knowledge, this is the smallest reflective type phase shifter at L-band, reported to date.**

## Introduction

Due to their low control complexity (only one control voltage), low loss, good stability against temperature changes and low sensivity on process tolerances, reflective type phase shifters (RTPS) are frequently used in radar systems. The first RTPS was introduced by [1] and has been improved by [2] and several other works. However, the compactness of these circuits is particularly limited by the size of the branch-line couplers, which use microstrip lines with lengths of λ/4. Recently, a work has been done to reduce the size of an L-band RTPS down to 12 mm x 60 mm by folding the microstrip lines of the coupler [3]. Nevertheless, these phase shifters still consume too large sizes for compact radar systems. A C-band GaAs MMIC RTPS has been reported in [4], for which the size was reduced to 3.6 mm x 1.6 mm.

The major design issue of our work was to further reduce the RTPS size by substituting the microstrip lines of the branch line coupler by lumped element equivalents [5]. To our knowledge, the RTPS presented here has the smallest size at L-band, reported to date, independent of the applied MMIC technology.

## Circuit Design

The RTPS was fabricated using the Triquint TQTRx GaAs MMIC process. The circuit topology of the designed RTPS is shown in Fig. 1. Input and output, which are matched to 50 Ω, are symmetrical. Instead of microstrip lines, the 90° 3 dB branch-line coupler is realized with lumped elements, which can be calculated as follows [6]:

$$C_1 = \frac{1}{2\pi f Z} \tag{1}$$

$$L_1 = \frac{Z}{2\pi f \sqrt{2}} \tag{2}$$

$$C_2 = \frac{1}{(2\pi f)^2 L_1} - C_1 \tag{3}$$

with port impedance Z and frequency f.

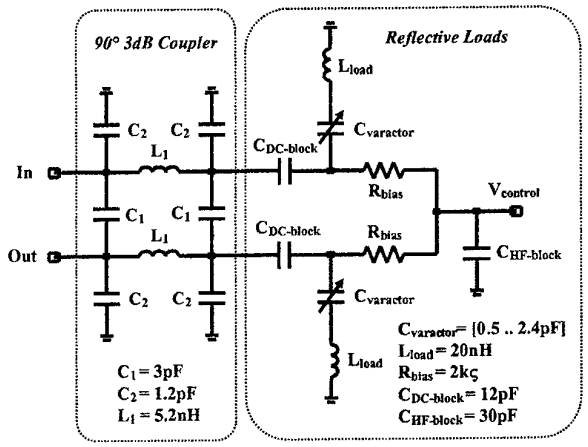


*Fig. 1: Circuit topology of the RTPS using lumped elements.*

The reflective loads consist of varactor diodes ($C_{varactor}$), which are resonated by inductors ($L_{load}$). Simulations have been performed in HP SERIES IV using a modified TOM II model [7] for the MESFET varactors and S-parameter files for the inductors. Inductors have been optimized using Sonnet [8]. The inductors $L_1$ and $L_{load}$ have line thicknesses of 6 µm, spacings of 5 µm and line widths of 15 µm and 5 µm, respectively. The varactor diodes are realized using deep depletion MESFETs (gate width = 1000 µm, gate length = 0.6 µm) with the drain and the source connected together. The phase of the circuit can be adjusted by the control voltage $V_{control}$, which is fed through the bias resistors $R_{bias}$.

A photography of the MMIC RTPS, mounted on a duroid test substrate, is shown in Fig. 2. The size is 0.85 mm x 1.1 mm.

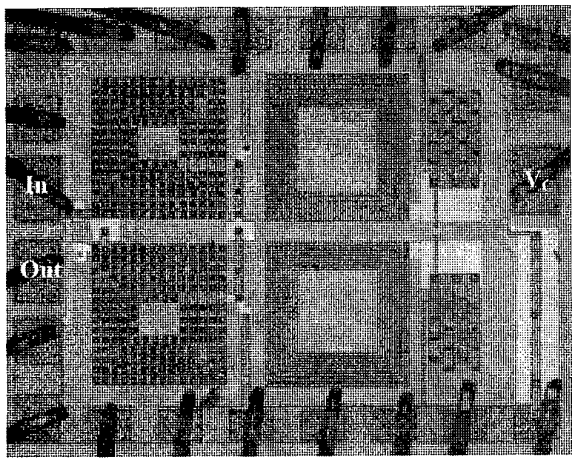


*Fig. 2: Photograph of the RTPS MMIC, chip size is 0.85 mm x 1.1 mm.*

## Measurements

Fig. 3 shows the phase shift, the signal loss and the input and output return loss versus control voltage at 1.2 GHz. A signal loss of -4.6 dB 61 dB and return losses of higher than 12.5 dB are measured within a phase control range of 210°.

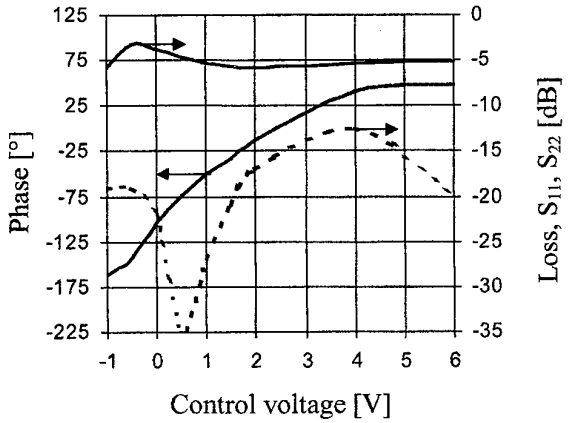


*Fig. 3: Measured phase (solid line), signal loss (solid line) and return losses (dotted) versus control voltage, f=1.2 GHz.*

Fig. 4 shows the large signal performance of the circuit. Within the 210° phase control range, the 1 dB compression point is higher than 7 dBm.
Within a bandwidth of 50 MHz, centered at 1.2 GHz and within a phase range of 210°, $S_{11}$ and $S_{22}$ are less than -12 dB and the signal loss variations are smaller than 6 0.5 dB.

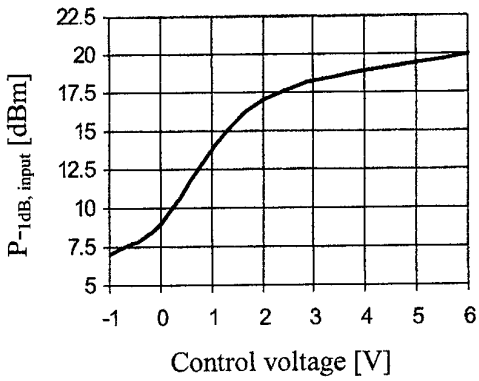


*Fig. 4: 1 dB input compression point versus control voltage.*

## Conclusion

A reflective type phase shifter MMIC at L-band has been presented, which has been designed for an aero navigation radar system. The circuit has an excellent large signal performance and allows a continuously adjustable 210° phase shift with moderate signal loss and high return losses. By using a 90° 3 dB coupler with lumped elements instead of microstrip lines, the circuit size has been significantly reduced in comparison to former approaches. To our knowledge, the presented circuit is the smallest reflective type phase shifter at L-band, reported to date.

### References


[1] R. N. Hardin, E. J. Downey, J. Munushian, *"Electronically variable phase shifter utilizing variable capacitance diodes"*, Proc. IRE, Vol. 48, May 1960, pp. 944-945.

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# Monolithic Integration of Optoelectronic III/V Devices with Silicon-Microelectronics

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Technical University Braunschweig, Hans-Sommer-Str. 66, D-38106 Braunschweig, Germany

A major impediment to the introduction of optical fiber communication to the subscriber area is the lack of inexpensive and mass-produced optoelectronic converters. Such a device should make use of the highly developed microelectronics on silicon and of the optoelectronic potential of III/V-compound semiconductors. The latter generally are of a direct electronic band structure so that they can be utilized as light emitters, in contrast to the indirect Si.

In this contribution we report on the monolithic integration of optoelectronic III/V devices together with MOS circuits in Si with (100) crystallographic orientation which is commonly used in industry. Because of its potential for mass-production we employ the metal-organic vapour-phase epitaxy to deposit the III/V-semiconductor films. We conduct our fabrication process in such a way that the production steps typical for III/V alloys do not unfavourably interfere with the Si technology, i.e. we fabricate the MOS circuits first, excluding the metallisation, after which the III/V devices are made. Finally, the metal interconnection is established.

We demonstrate the feasibility of our process by a metal-semiconductor-metal (MSM) photodetector on the basis of InGaAs which is monolithically integrated with a 3-stage MOS amplifier on a Si substrate (cf. Fig.1). To accommodate the mismatch of the lattice constant of the Si substrate and the InGaAs photodetector fitted to InP (about 8 %) we placed a sequence of GaAs and InP films as well as an InGaAs/InP superlattice in between.

Our experiments show that the performance of the MOS circuits do not deteriorate when they are subjected to the high-temperature steps of the epitaxial growth. The amplification factor is 27 and 34 db with or without this heat treatment, respectively. The corresponding figures for the 3-db roll-off frequency are 143 and 98 kHz. The characteristic features of the photodetector (dark current, illumination sensitivity) do not differ from each other substantially whether the device is produced on a Si substrate or on the native substrate InP.

The crucial test for any integration on a Si substrate is the proof of efficient electroluminescence. We present measurements of light emission at a wavelength of about 1.5 µm of a

large-area surface-emitting LED. The comparison of the same device structure, but made on an InP substrate, reveals that in the high-current regime the emission is reduced only by a factor of about 3 on the Si substrate. In the latter case, no emission saturation due to heat dissipation is observed since the thermal conductivity of Si is much larger than that of InP. In addition we investigated the emission of a ridge-waveguide type of laser structure. If the dimensions of the device will be reduced our results suggest that cw laser action can be expected. Such a reduction of the lateral dimensions can be achieved by area-selective epitaxy. It offers the additional advantage of fewer threading dislocations which penetrate the epitaxial film at an angle of 60°.

The intention of our experiments is to show that the III/V technology can be incorporated in the well-established Si processes, i. e. the former has to be adapted to the requirements of the latter. Therefore, our devices have relatively large dimensions. If state-of-the-art submicron devices are employed unwanted outdiffusion might occur due to the high temperatures during the epitaxial growth of the III/V-semiconductor layers.

We conclude by a discussion of the diffusion effects which can be expected in an advanced 0.4 µm CMOS process when the thermal load of the epitaxial III/V-crystal growth is applied. The result is that the thermal budget can be kept constant if appropriate annealing steps during CMOS fabrication are postponed to the epitaxy.


Fig. 1: SEM photograph of interdigitated MSM photodetector (enlarged upper right) monolithically integrated on (100)Si with 3-stage MOS-amplifier (left part).

# Monolithically Integrated Traveling-Wave Amplifier for Low-Cost Broadband Optical Receiver

A. Orzati, Student Member, IEEE, W. Bächtold, Fellow, IEEE

*Abstract* — **A monolithically integrated traveling-wave amplifier (TWA) has been designed and fabricated using the commercial GaAs TQTRx 0.6μm process, showing 10dB gain from DC to 12GHz and an open eye-diagram for 10Gb/s NRZ digital transmission. Cascode cells have been used as amplifying stages. Size reduction has been obtained by substituting the input and output transmission lines with LC networks. This amplifier is a good candidate as front end in a low-cost broadband optical receiver.**

*Index Terms* — **TWA, broadband amplifier, MMICs, optical communication system.**

## I. Introduction

High-speed receivers for multi-gigabit optical communication systems have been increasingly needed in the last years. The front-end amplifier represents a key component of the receiver. Therefore it is becoming a market issue to design and fabricate low-cost, broadband amplifiers for this application. The goal of this work was to indicate that the traveling-wave amplifier topology is a suitable candidate for a 10Gb/s front end in low-cost optical communication systems. For this reason a commercial low-cost high-yield GaAs process like the TriQuint TQTRx was chosen. At a cost of 0.8 US$/mm$^2$ for mass production, this process provides 0.6μm E-FETs with a $f_t$ of around 18GHz and high-Q inductors.

## II. Circuit Design

The schematic of the designed circuit is shown in Fig.1. It is a classical traveling-wave amplifier topology ([1]-[4]) consisting of an input and output line both terminated with a resistor, and cascode circuits as gain cells. An input voltage is applied at the input line terminal and travels down to its terminated end where it is absorbed by the resistor. As the voltage wave propagates, the different amplification stages are excited and the signal is amplified and transmitted to the output line where two voltage waves are generated in opposite directions. If the phase velocities of the input and output line are the same then the voltages traveling in the forward direction on the output line add in phase. The signal components traveling in the opposite direction add not in phase and the remaining components are absorbed by the output line termination. Cascoded transistors were used for two main reasons. First, this configuration shows significantly higher maximum available gain at high frequencies compared to a single transistor. Second, its highly increased output resistance drastically lowers the output-line losses, thus increasing the overall frequency performance of the amplifier.

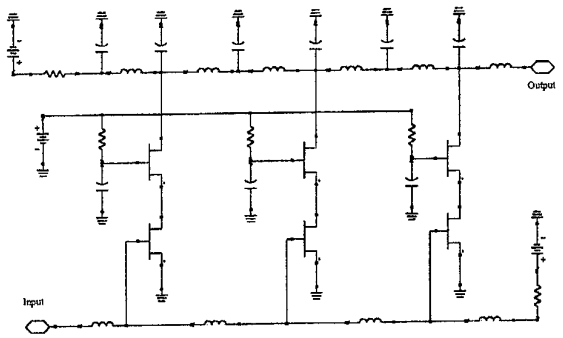


Figure 1: Schematic of the designed TWA.

The drawback of most traveling-wave amplifiers is the large chip size, in most cases due to the considerable dimensions of transmission lines in the circuit layout. For this reason, lumped elements were used in the synthesis of the input and output line, thus reducing the required chip size. By choosing the appropriate transistor geometry, the input transmission line could be realized using only 1.3nH spiral inductors together with the input capacitance of the cascode cell [5]. Due to the high inductance values required, the same approach could not be used for the output line, hence capacitive elements had to be added. The line terminations do not exactly match the in and output line impedance (50Ω). This causes reflections, thus deteriorating the return losses, but results in a flatter frequency response.

The layout of the fabricated circuit is shown in Fig. 2. The total chip size is 1.36 mm$^2$, corresponding in a mass production cost of around 1US$. The supply voltage is 4V and the total DC current is 19mA.

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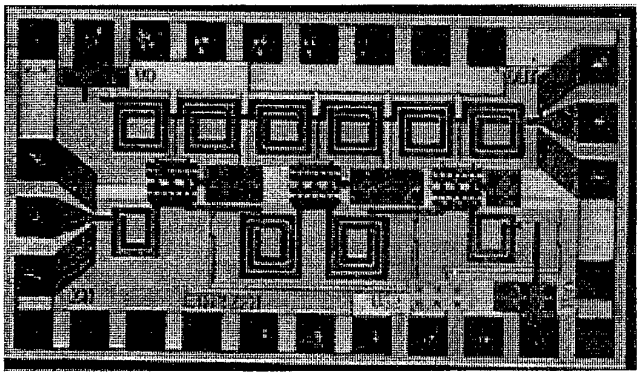

Figure 2: Photograph of the fabricated circuit.

## III. Results

After fabrication, characterization of the circuit was performed. S-parameter measurements were carried out using a HP-8510B network analyzer. As it can be seen from the measurement results in Fig.3, the amplifier shows around 10dB gain up to 10GHz and has acceptable performances up to 12GHz. The flat frequency response and the very good return loss measurements at both input and output ports give this amplifier the possibility to be successfully used in cascaded amplification chains.

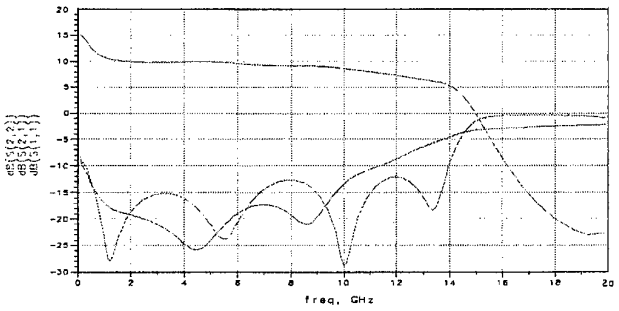


Figure 3: Measured S-parameters of the amplifier.

In order to have a full characterization of the component eye-diagram measurements for a 10Gb/s NRZ signal were performed. The measurement result is reported in Fig. 4.

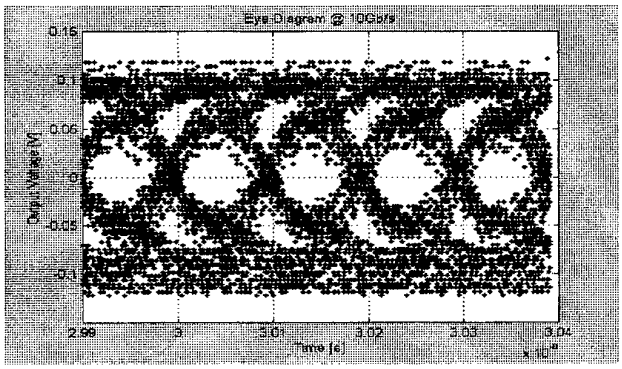


Figure 4: Eye-diagram for a 10Gb/s NRZ signal.

The eye-diagram shows a good opening and demonstrates the suitability of this amplifier as an optical receiver front-end for a 10Gb/s optical communication system. This result has been achieved due to the excellent broadband performance of the traveling-wave topology.

## IV. Conclusions

In this paper a DC-12GHz traveling-wave amplifier has been designed and fabricated using a low-cost high-yield commercial GaAs process. The TWA topology was implemented using lumped elements instead of the traditional transmission lines. S-parameter and eye-diagram measurements showed that this amplifier is suitable as a receiver front end in an optical communication system. To the author's knowledge this is the first work presenting a DC-12GHz traveling-wave amplifier fabricated on a low-cost high-yield GaAs MESFET process, using lumped elements instead of transmission lines.

## Acknowledgments

The author would like to thank Hansruedi Benedickter and Iwan Schnyder for helping in the characterization of the amplifier and Thomas Brauner for fruitful discussions.

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## III-V material and device aspects for the monolithic integration of GaAs devices on Si using GaAs/Si low temperature wafer bonding

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### ABSTRACT

A new process for wafer scale integration of GaAs devices on Si has been investigated. The process is based on low temperature bonding of epitaxial GaAs to Si wafers, either plain Si substrates or planarized fully processed CMOS wafers. The method is especially suitable for monolithic integration of high quality GaAs optoelectronic interconnects (O/Is) on Si CMOS chips and its development was undertaken within the ESPRIT MEL-ARI OPTO project BONTEC.

We will describe the basic process flow and will present the most important aspects of the work concerning the III-V material and devices, which was required to demonstrate the feasibility of this new GaAs-Si integration process. The low temperature wafer bonding is very demanding for the design, growth and processing of the III-V epitaxial structures. There are very strict requirements on the morphological characteristics of the epitaxial GaAs wafer, i.e. a flat surface without any protruding defects or layer steps is needed. In Molecular Beam Epitaxy (MBE) growth, this practically means that a single growth (no regrowth) is required and special care is needed to eliminate hillock type oval defects and any other epitaxial spikes. The GaAs/AlGaAs device heterostructures are grown with an inversed epitaxial structure on GaAs, after the inclusion of an AlAs etch stop layer. Following GaAs-Si wafer bonding, backside thinning of the GaAs substrate is used in order to leave a thin epitaxial heterostructure on Si, which is then processed into III-V devices. Thinning is performed using chemical mechanical polishing (CMP) or wet etching to remove most of the substrate, and RIE dry etching to selectively remove the remaining GaAs material without affecting the heterostructure that is protected by the AlAs etch stop layer.

Our III-V work has addressed these issues. Good bonding was achieved by eliminating the hillock - type oval defects created during MBE growth. The performance capabilities of both laser diode (LD) and photodiode (PD) devices fabricated from a unique multiple quantum well (MQW) GaAs/AlGaAs LD structure with 2-32 QWs were determined. Cleaved mirrors LDs (Fig. 1), non-guided wave and guided wave PDs were fabricated and measured, for structure optimization. A structure with 4 QWs was selected for demonstrating the integrated O/Is on Si. A $BCl_3$ reactive ion etching (RIE) process was developed and lasers with RIE mirrors were fabricated, exhibiting typical threshold current density values around 1.6 KA/cm$^2$ with best results being less than 1 KA/cm$^2$. The process was applied successfully on bonded GaAs structures and integrated LDs and PDs were fabricated on Si (Figs. 2, 3) with similar performance characteristics to reference devices fabricated on GaAs substrates. Various test devices and structures, including GaAs MESFET transistors, were also integrated on Si using the same bonding process and were studied to provide a more general understanding of the process.

**Acknowledgments:** EU has supported this work through ESPRIT 28998 project "BONTEC".

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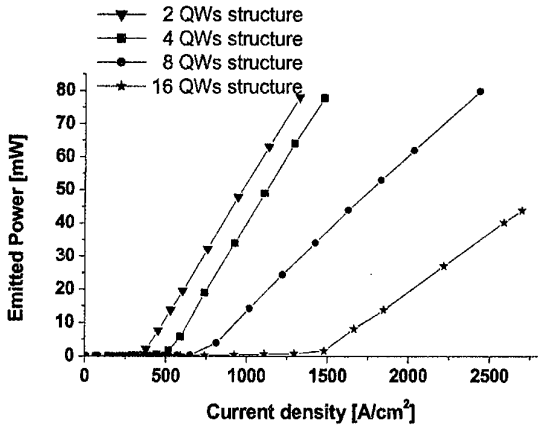


***Figure 1****.Emitted optical power of 50x400 micron broad area lasers with cleaved mirrors, fabricated from GaAs/AlGaAs GRINSCH structures with 2, 4, 8 and 16 QWs.*

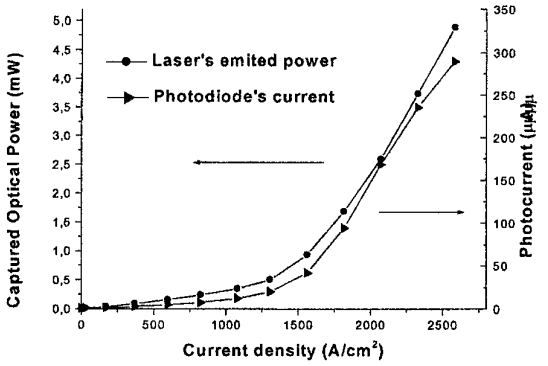


***Figure 2****. Emitted power of a 10x250 micron laser diode with etched mirrors fabricated from a GRINSCH structure with 4 QWs and response of the photodiode for a laser diode - photodetector system. All components are realized using the same structure.*

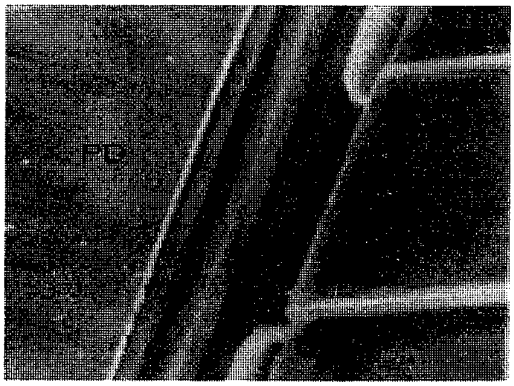

***Figure 3****. SEM view of integrated GaAs optoelectronic devices, fabricated by the $BCl_3$ RIE-based process.*

# INFLUENCE OF THE INTEGRATION ON THE PERFORMANCE OF BIDIRECTIONAL MODULES FOR SINGLE FIBER APPLICATION

**Heinz-Christoph Neitzert * and Agnese Piccirillo #**

* Università di Salerno, DIIIE, Fisciano, Italy, # Telecom Italia Lab, Torino, Italy

Optical access network components need to operate in uncontrolled environments. In particular the sensitivity of their performance to temperature variations is of great interest. A key component for full duplex operation over a single optical fiber, as foreseen in a passive optical network (PON)[1], is the bidirectional (BIDI) optoelectronic module. While there is an ample literature regarding the temperature dependence of the optoelectronic emitter performance, in particular of 1300nm Fabry-Perot (F-P) lasers [2,3], the temperature dependence of other BIDI device parameters is less documented. While most commercially available BIDI modules are micro-optic type devices, there are strong efforts to develop low-cost integrated devices [4,5,6].

Here we compare 32 BIDI modules with different degree of integration, which can be classified in 6 different categories (see Table 1), depending on the type of optical interconnect technology and emitter and receiver wavelength allocation. Most devices were micro-optic (Mo) modules, that means that emitter and receiver contained in different TO-like packages were assembled with micro-optic components. Additionally we also measured BIDI's were emitting and receiving functions were assembled on a single silicon optical bench (SiOB) and first commercial BIDI devices using planar waveguide technology (PLC). Parameter extraction during temperature cycling tests (between -40°C and +85°C) enabled a rapid evaluation of the temperature behaviour and stability of the different modules. A complete temperature cycle lasted about 100min (Fig.1) and only a small hysteresis was found between the values of the parameters extracted during increasing and decreasing temperature ramps (see Fig.2). The measured coefficients of the wavelength change vs. temperature for the modules with lasers emitting around 1550nm were all within a small range between 0.53nm/K and 0.58nm/K, while for the 1300nm emitting devices values between 0.26nm/K and 0.47nm/K have been observed. Comparing these values to the FSAN specifications [7] (1260-1360nm window and 1480-1580nm window), it can be stated that the maximum permitted wavelength change within the –40°C to +85°C temperature range can be met by all modules if the room temperature wavelength has been selected properly.

In Table 1 the optical crosstalk (OCT) and the fiber coupled receiver responsivity (R) at 25°C, the optical backreflection (OBR) at 1300nm and at 1550nm and the tracking error (TE) of the optical power for constant monitor diode current for the different types of bidirectional modules are given. Most striking are the low fiber coupled responsivities of the planar waveguide devices, due to coupling losses between the waveguides and the optical fiber or receiver diode chip. The tracking error of most modules was - independent of the type of technology - below the usually specified 1dB margin within the whole temperature range. A comparison of the single wavelength modules with different technologies shows that the PLC type modules have about 10dB higher optical crosstalk values compared to the micro-optic devices. In the case of the WDM modules, the mean values of the micro-optic module crosstalk is about 20dB lower than the optical crosstalk of the silicon optical bench (SiOB) modules. In Fig.3 it can be seen that for all types of characterized modules the crosstalk did not vary significantly with temperature. Comparing the emitting properties of a large number of Fabry-Perot lasers from different manufacturers (Fig.4) we observed a strong correlation between the values of the laser threshold currents and the characteristic temperatures independent of the emitting wavelength (1300nm and 1550nm). This means that there is a tradeoff between low theshold currents and good high temperature behaviour for these lasers.

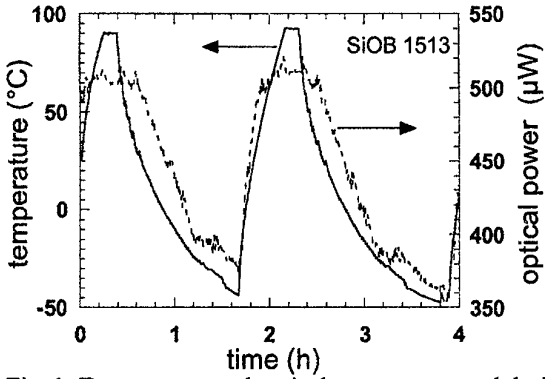


Fig. 1: Temperature and optical power measured during temperature cycling with constant monitor current of a Silicon optical bench BIDI module

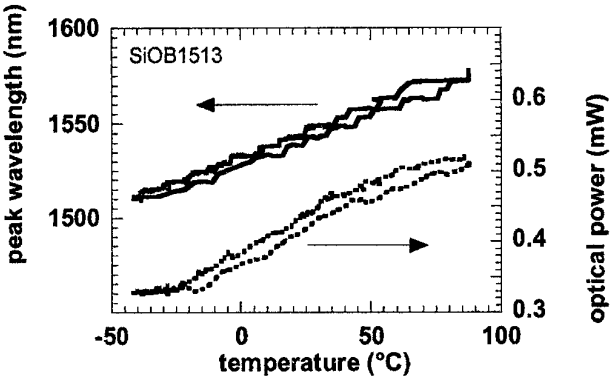


Fig. 2: Temperature dependence of the emitting wavelength and optical power of a SiOB module

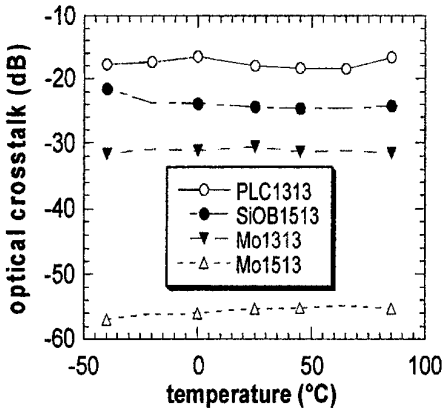


Fig.3: Temperature dependence of the optical crosstalk of different types of bidirectional modules

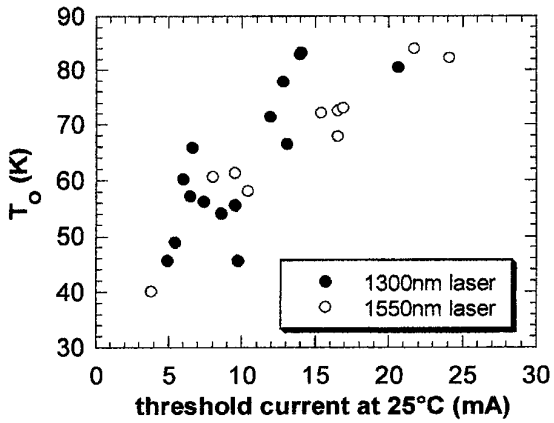


Fig. 4: Characteristic temperature of different BIDI F-P lasers as a function of the 25°C threshold current

| Module type | OCT (dB) at 25°C | TE (dB) - 40...+85°C | R (A/W) at 25°C | OBR(dB) at 1300nm | OBR (dB) at 1550nm |
|---|---|---|---|---|---|
| Mo1313<br>Mo1315<br>Mo1513 | -27.5 / -30.6<br>-42.0 / -71.1<br>-48.9 / -57.3 | 0.26 / 0.58<br>0.43 / 1.00<br>0.28 / 0.99 | 0.30 / 0.35<br>0.52 / 0.79<br>0.55 / 0.85 | -14.3 / -19.7<br>-10.0 / -12.8<br>-51.1 / -74.7 | -17.2 / -18.6<br>-19.7 / -62.5<br>-6.4 / -17.7 |
| SiOB1315<br>SiOB1513 | -27.5<br>-24.3 | 1.06<br>1.34 | 0.57<br>0.46 | -15.5<br>-56.4 | -56.4<br>-19.8 |
| PLC1313 | -16.4 / -18.0 | 0.43 | 0.10 / 0.13 | -39.2 | |

Table 1: Optical crosstalk, tracking error, responsivity and optical back reflection of different types of BIDI modules

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# SESSION II
# Heterojunction Bipolar Transistors
# Chair: Prof. Dimitris Pavlidis
# Monday May 28, 2001

| | |
|---|---|
| **10.45 am**<br><br>**INVITED** | **GaInP-GaAs HBT's for High Frequency and High Power Applications**<br>*S.L. Delage, D. Floriot, S. Cassette, N. Caillas, E. Chartier, N. Frapsauce, M. Surrugue, J.C. Jacquet, S. Piotrowicz, M.A.diForte-Poisson*<br>THALES LCR (formerly Thomson-CSF/LCR) Domaine de Corbeville, F-91404 Orsay Cedex |
| **11.10 am** | **InSb Heterostructure Bipolar Transistor Operating at Room Temperature**<br>*T. J. Phillips, T. Ashley, T. M. Burke and A. B. Dean*<br>DERA, St Andrews Road, Malvern, WR14 3PS, UK |
| **11.25 am** | **Carbon Doped InP/InGaAs-HBT: Consistent Small-Signal and RF-Noise Modelling and Characterization**<br>*M. Agethen, S. Schüller, P. Velling, W. Brockerhoff, F.-J. Tegude*<br>Solid-State-Electonics Dept. Gerhard-Mercator-University Duisburg, ZHO / LT 207, Lotharstrasse 55, D-47057 Duisburg, Germany |
| **11.40 am** | **Influence of the Emitter Orientation on the Current Gain of InP/InGaAs DHBTs**<br>*I. Schnyder, M. Rohner, and H. Jäckel*<br>Electronics Laboratory, Swiss Federal Institute of Technology, CH-8092 Zurich, Switzerland |
| **11.55 am** | **High speed fully self-aligned collector-up MHBTs**<br>*S. Demichel[(a)], R. Teissier[(a)], F. Pardo[(a)], F. Mollot[(b)] and J-L. Pelouard[(a)]*<br>(a) LPN-CNRS, 196 Av. H. Ravera, BP 29, 92222 Bagneux Cedex – France<br>(b) IEMN, Avenue Poincarré, BP 69, 59652 Villeneuve d'Ascq – France |
| **12.10 am** | **Highly Efficient GaInP/GaAs HBTs for High Power Applications**<br>*J. Würfl[(a)], P. Kurpas[(a)], R. Doerner[(a)], B. Janke[(a)], P. Heymann[(a)], A. Maaßdorf[(a)], W. Doser[(b)], P. Auxemery[(c)], H. Blanck[(b)], D. Pons[(c)], W. Heinrich[(a)]*<br>a) Ferdinand-Braun-Institut (FBH), D-12489 Berlin – Germany<br>b) ums GmbH, D-89081 Ulm – Germany<br>c) ums Orsay, F-91404 Orsay Cedex – France |
| **12.25 am** | **Design Optimisation of InP/InGaAs HBTs**<br>*A.A. Rezazadeh[(a)] and H Sheng[(b)]*,<br>(a) Department of Electronics Engineering King's College London, Strand, London. WC2R 2LS, UK.<br>(b) Current Address: NortelNetworks. NORTEL Networks, Ottawa, Ontario, CANADA |

## GaInP-GaAs HBT's for High Frequency and High Power Applications

S.L. Delage, D. Floriot, S. Cassette, N. Caillas, E. Chartier, N. Frapsauce, M. Surrugue, J.C. Jacquet, S. Piotrowicz, M.A.diForte-Poisson

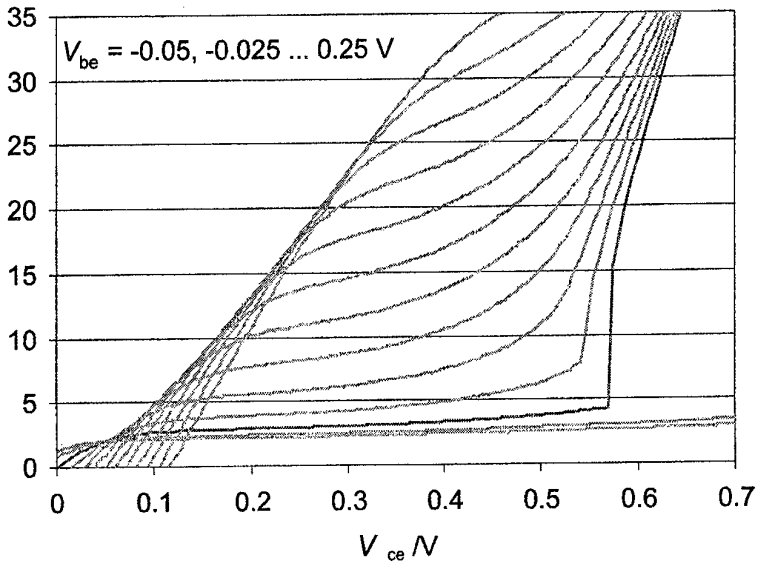
**THALES LCR** (formerly Thomson-CSF/LCR) Domaine de Corbeville, F-91404 Orsay Cedex

HBT technology is now considered a mature technology for mobile phone applications. Those applications below 2GHz require medium power level not exceeding 2W and low DC bias. HBT technologies for higher frequencies and power levels need to use higher current densities and DC bias. The impact on thermal management and reliability is therefore crucial. This paper will address an overview of the technologies to be developed to achieve reliable high efficiency integrated amplifiers above 3GHz and up to 20GHz.

# InSb Heterostructure Bipolar Transistor Operating at Room Temperature

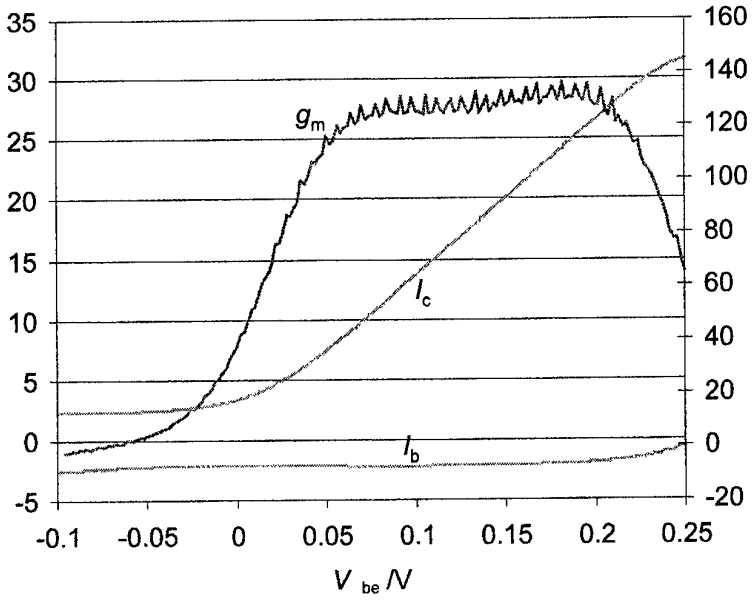
T. J. Phillips*, T. Ashley, T. M. Burke and A. B. Dean
DERA, St Andrews Road, Malvern, WR14 3PS, UK

We have previously demonstrated room temperature operation of InSb FETs using the technique of carrier exclusion/extraction [1]. In this paper we show that ambient temperature operation of bipolar devices can also be achieved.




## Introduction

The performance of transistors (both FET and bipolar) made from narrow bandgap semiconductors is limited by the effect of intrinsic carriers, which cause excess leakage in the off-state, and also contribute to impact ionisation. We have pioneered the use of carrier exclusion/extraction to reduce the carrier concentration in the active region of a device by many orders of magnitude. This technique has now been applied to bipolar devices [2].

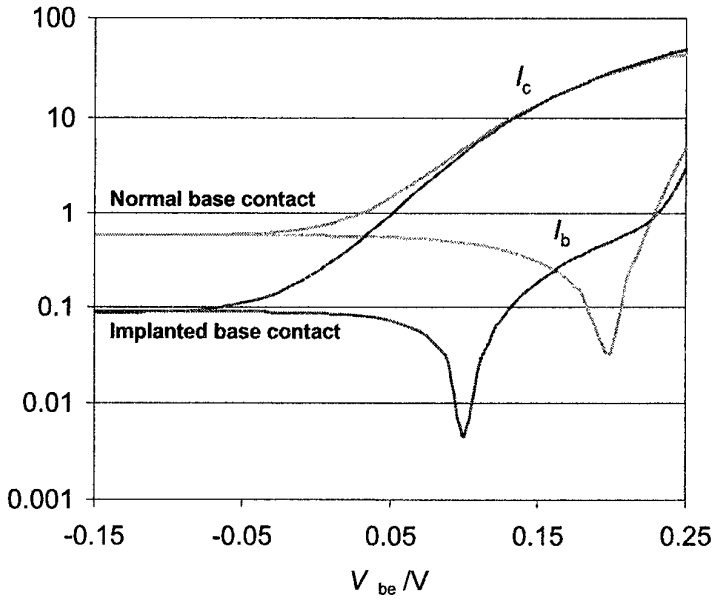


**Bipolar Device Design**

The device design is similar to a conventional bipolar design, with InSb used for all layers except for the emitter, which is made from $Al_{0.05}In_{0.95}Sb$ and provides a valence band barrier at the emitter-base junction. The base is highly p-type doped, but at present does not contain the $p^{++}$ implant that will provide the full carrier extraction benefit. However the base can still be reverse-biassed to extract carriers from (mainly) the low-doped collector region. The emitter size is 6 μm x 25 μm, and the collector size 22 μm x 25 μm.

**Device Results**

The resulting device shows low voltage output characteristics, with drain voltages up to 0.6 V and base voltages up to 0.25 V (0.05 V steps). The two lowest lines on the output characteristic are with a negative bias applied to the base, showing how the carrier extraction technique reduces leakage and suppresses breakdown (in fact at negative base voltages the device shows a breakdown voltage of over 1.2 V). The device also shows excellent transconductance, as shown in the characteristic above, limited at higher current by series resistance in the device, which needs optimising. The base-emitter diode shows a *reverse* current, even at positive base voltages, due to the removal of the thermally




generated carriers from the device, and passes through zero current at $V_{be} = 0.25$ V. Because of this, the differential current gain is very large (hence the output characteristic above is shown with base *voltage* as the parameter). AC measurements on these 6 μm emitter devices are very promising, showing an $f_T$ of over 25 GHz in a device not optimised for high speed performance.

**Modelling and Discussion**

Modelling shows that addition of a $p^{++}$ implanted base contact results in a factor of eight reduction in leakage current (see graph above). It also shifts the base-emitter turn-on voltage down towards zero. Scaling of the device leads to a predicted $f_T$ of over 600 GHz for devices with 1 μm emitters.

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# Carbon Doped InP/InGaAs HBT: Consistent Small-Signal and RF-Noise Modelling and Characterization

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## Abstract

InP/InGaAs-HBT are most interesting components for high gain, high speed and power applications. In this work a consistent small-signal and noise parameter model for these devices is presented. Different devices in three mesa technology are investigated, varying with respect to emitter, base and collector layer thickness and compositional base grading. Besides bias dependent characterization, temperature depending properties between 15K and 380K are investigated, too, by measurements as well as modelling. These studies based on a broad yet specific data base allows for correlating intrinsic device properties, like e.g. noise sources, to relevant device regions, thus supporting the physical understanding and improvement of design.

## 1 Introduction

In case of HBT rf-noise parameter modelling there are different approaches to model all high frequency noise parameters (minimum noise figure $F_{min}$, equivalent noise resistance $R_n$, and optimum generator reflection coefficient $\Gamma_{opt}$), which describe the rf-noise behaviour of the investigated device.

## 2 Physically Relevant Small-Signal and RF-Noise Parameter Model of HBT

Fig. 1 shows the physically relevant "T"-like consistent small-signal and rf-noise model of HBT based on the typical 3-mesa structure of HBT realised on InP [1]. To all resistances equivalent noise temperatures are associated. Adding only four intrinsic equivalent noise temperatures the rf-noise parameter modelling becomes possible. In addition these temperatures are correlated to specific device resistances as base-emitter as well as base-collector junction or base and collector sheet resistances. The contribution of the parasitic resistances is assumed to be thermal noise only, and therefore their equivalent noise temperature is equal to the ambient temperature $T_A$ during measurement. With the help of this model the small-signal as well as rf-noise behaviour of HBT devices can be described in the frequency range from 45 MHz up to 40 GHz and 2 GHz up to 18 GHz, resp.

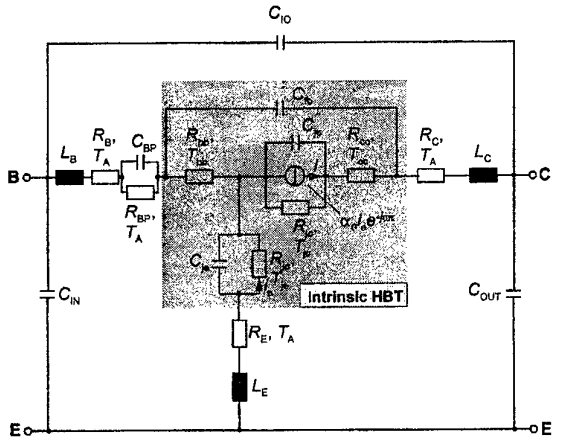


**Fig. 1:** The consistent small-signal and rf-noise equivalent circuit of the HBT.

## 3 Investigated Devices and Results

Devices under test are carbon doped InP/InGaAs non self-aligned HBT with an emitter area $A_E = 30\mu m^2$, grown by LP-MOVPE with non gaseous sources (TBAs/TBP, DitBuSi/CBr4, TMIn/TEGa) in nitrogen carrier gas. The InGaAs base layer is carbon doped ($p > 10^{19} cm^{-3}$) and a high temperature in-situ annealing sequence is carried out in TMAs/N2 ambient at $T > 600°C$ to activate the carbon doping in the base. Tab. 1 gives an overview of the layer sequences of investigated devices.

**Tab. 1:** Layer sequences of the investigated devices

| | **Layer width *t*/ nm** | | |
|---|---|---|---|
| | ***M1965*** | ***M2000*** | ***M2005*** |
| E-Cap | 135 | 135 | 135 |
| Emitter | 65 | 65 | 65 |
| Base | 70 | **140** | **140** |
| Collector | 270 | 270 | **200** |
| Sub-Collector | 270 | 270 | 270 |

Bias and temperature dependent rf-measurements are performed for all devices and will be presented during presentation. To compare the rf-noise performance of the HBT, the results of measured and modelled noise parameters at room temperature will be shown for identical bias condition in active device region (collector-emitter voltage $V_{CE} = 1.2$ V and collector current $I_C = 10$ mA). Fig. 2 shows the influence of the layer widths on the minimum noise figure $F_{min}$. With rising layer widths, the values of the minimum noise figure increases. The strongest influence is obvious looking on the base width, the minimum noise figure

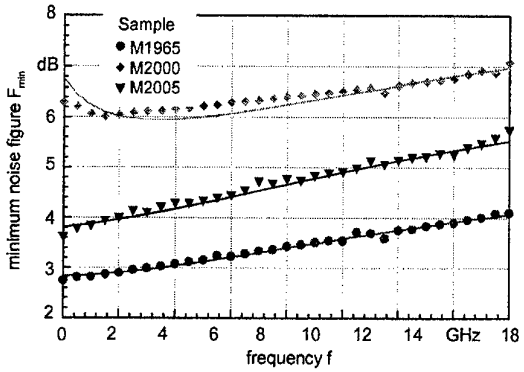


**Fig. 2:** Minimum noise figure $F_{min}$ for various HBT samples.

increases drastically with wider base layer (M2000 and M2005).

The same strong influence of the base width on rf-noise parameter is obvious for the equivalent noise resistance $R_n$, too (fig. 3). If the base width is high, $R_n$ increases. But with smaller collector width, the lowest values of $R_n$ are achieved (M2005).

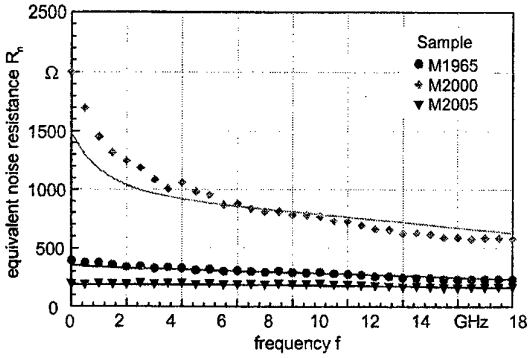


**Fig. 3:** Equivalent noise resistance $R_n$ for various HBT samples.

The HBT with lowest collector width show the smallest magnitude of optimum generator reflection coefficient $\underline{\Gamma}_{opt}$ (fig. 4).

Evolutionary optimisation algorithm in combination with multi-bias approach are used to determine the small-signal parameter as well as the equivalent noise temperature of the consistent model [2]. The lines in the above given figures represent the modelled data, which describe all measured entities very well.

## 4 Intrinsic Noise Sources

As a result of the above mentioned small-signal and rf-noise parameter model a localization of various noise sources in the specific device regions is possible. With the parameter extraction results, the spectral densities of the four intrinsic noise current sources can be calculated with formula (1) and investigated in dependence on bias condition, here in dependence on shot noise currents due to dc device currents $I_B$ and $I_C$. The resistance $R_x$ and equivalent noise temperature $T_x$ represent the various intrinsic noise sources.

To demonstrate the bias dependent behaviour of the intrinsic noise sources, Fig. 5 shows as an example the

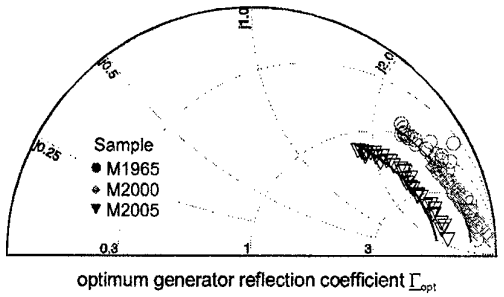


**Fig. 4:** Optimum generator reflection coefficient $\underline{\Gamma}_{opt}$ for various HBT sample.

$$i_{x,n} = \sqrt{4k\frac{T_x}{R_x}}\,, \qquad (1)$$

intrinsic base noise current $i_{bb,n}$ in dependence on base current shot noise. This noise source shows an linear dependence on the base current shot noise, but includes an high offset. The gradient and this offset have to be investigated in more detail. The other intrinsic noise sources are identical to base or collector dc current shot noise.

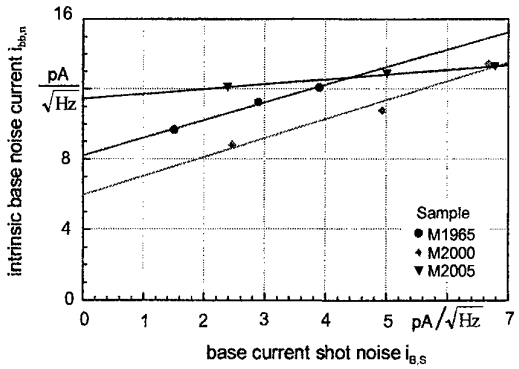


**Fig.5:** Intrinsic base resistance noise source current $i_{bb,n}$ in dependence on base current shot noise $i_{B,S}$ for various HBT samples.

## 5 Conclusion

A consistent small-signal and rf-noise parameter model for InP based HBT is presented. The advantage of this model is the physical relevance using the "T"-like model and the correlation of intrinsic noise sources to specific device regions.

## 6 Literature


[1] J.S. Yuan, "SiGe, GaAs, and InP Heterojunction Bipolar Transistors", Wiley-Interscience, John Wiley & Sons, Inc., New York

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# Influence of the Emitter Orientation on the Current Gain of InP/InGaAs HBTs

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## Introduction

One of the major problems of self-aligned InP HBTs is their relatively low current gain $\beta$. In [1] we stated that the current gain can be improved by choosing a larger distance between the base-emitter junction and the base contacts. In this paper we explain the physical mechanisms responsible for this effect [2].

## Devices - Experimental Results

For our analysis we used both InP/InGaAs DHBT [1] and SHBT [3] devices with the identical epitaxial base-emitter layer structure. Aligning both device types (DHBTs and SHBTs) along the [010] (diagonal) and the [01$\bar{1}$] (horizontal) direction on a (100) InP substrate, two different geometries for the emitter mesa were obtained (see Figure 1). For a horizontal SHBT the emitter undercut $Y_e$ was measured $\sim 20$ nm, for a diagonal SHBT it was measured $\sim 400$ nm. The measured Gummel plots of these two geometries for a SHBT layer structure show identical collector current densities while the base current densities differ by more than one order of magnitude at low bias (see Figure 2). The current shift in Figure 2 is due to different effective base emitter junction areas and different base access resistance caused by the two different emitter geometries. The change in base current between the diagonal and the horizontal geometries is also observed for DHBT devices.

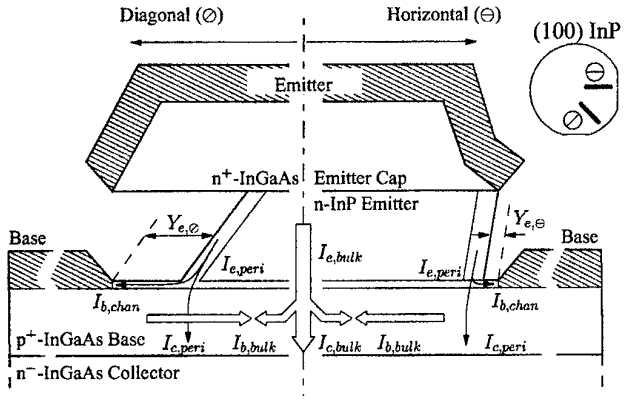


Figure 1: Schematical cross-sections of HBTs with horizontally (labelled with the subscript ⊖) and diagonally (labelled with the subscript ⊘) emitters.

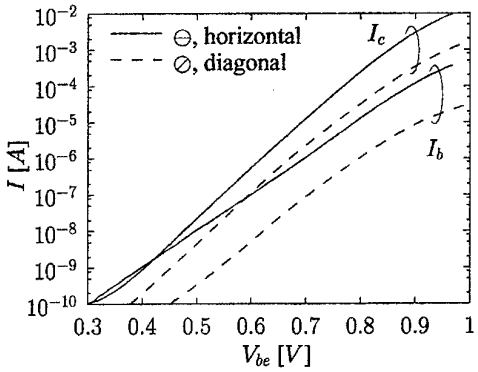


Figure 2: Comparison ot the measured Gummel plots of transistors with the two different emitter orientations.

## Theory

To explain the correlation between emitter undercut and current gain degradation, two physical mechanisms have to be taken into account: (a) surface states at the emitter sidewall and (b) surface states at the extrinsic base surface. As shown in [4], surface states at the emitter sidewall cause a Fermi level pinning close to the neutrality level $E_{H0}$ along the emitter sidewall (see Figure 3). At low bias, this Fermi level pinning causes an electron accumulation, which increases the perimeter emitter current $I_{e,peri}$ in Figure 1 along the emitter sidewall. At high bias, the emitter surface becomes depleted. In that case the whole emitter current flows in the emitter bulk region ($I_{e,bulk}$, bulk emitter current). Surface states at the extrinsic base surface [5] form a conducting channel between the base-emitter junction and the base contacts in which the channel base current $I_{b,chan}$ flows in parallel to the bulk base current $I_{b,bulk}$.

It is the combination of these two mechanisms in case of low bias which degrades the current gain $\beta$: Electrons which flow along this emitter sidewall ($I_{e,peri}$) enter the base and become trapped in the conductive base surface channel because of

their low kinetic energy, thereby contributing to the channel base current $I_{b,chan}$. Using 2D drift/diffusion and Monte Carlo simulations, the measured influence of these two mechanisms on the current gain could be reproduced [2]. The channel base current $I_{b,chan}$ can be reduced by more than one order of magnitude by enlarging the emitter undercut by aligning the devices along the diagonal direction [2]. The drawback of an enlarged emitter undercut ($Y_{e,\ominus} \sim 20$ nm vs. $Y_{e,\oslash} \sim 400$ nm in our case) is a small loss of RF-performance ($f_{max}$) because of an increase of the base access resistance by $\sim$ 10-20 %, depending on the base layer sheet resistance.

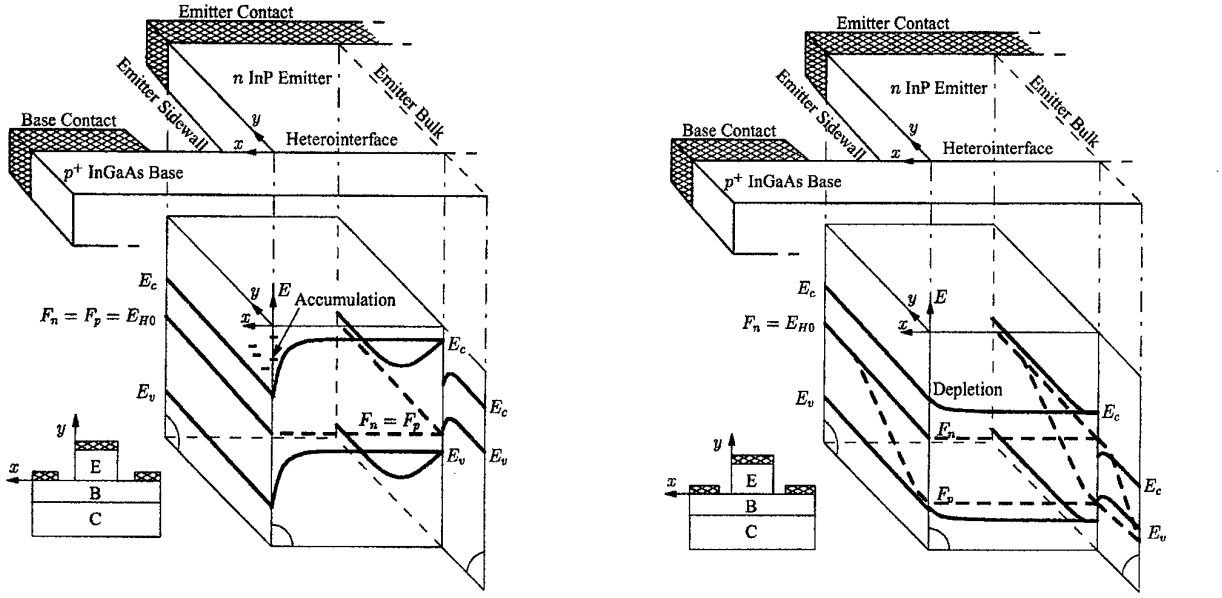


Figure 3: Band diagrams in a schematical HBT: along the emitter sidewall, in the emitter/base bulk and along the base emitter heterointerface. On the left: low bias case ($V_{BE} = 0$ V), on the right: high bias case. ($E_c$: conduction band; $E_v$: valence band; $F_n$: electron Fermi level; $F_p$: hole Fermi level; $E_{H0}$: charge neutrality level)

## Conclusion

An analysis of current gain degrading mechanisms for InP/InGaAs HBTs was carried out. We found that the combination of two effects is responsible for the current gain degradation at low bias [2]. The influence of these effects on the current gain $\beta$ can be reduced providing a larger emitter undercut either by aligning the emitter mesa diagonally along the [010] direction on a (100) wafer or by other processing techniques. The resulting increase of the base access resistance is thereby the main drawback for our specific devices, which are not optimized yet. Analysis of more samples with different emitter undercuts and further optimization will be required to obtain the optimal tradeoff between the current gain $\beta$ and the base access resistance of the device, and to examine the reproducibility of the emitter undercut.

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# High speed fully self-aligned collector-up MHBTs

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InP-based heterojunction bipolar transistors (HBT) have already shown great potential in high-speed electronics due to their excellent high-frequency characteristics[1]. However further advances in HBT design and technology are necessary to improve their performance and respond to the needs in high-speed circuits such as those for high bite rate optical telecommunications (160 Gbit/s or faster).

The Metal Heterojunction Bipolar Transistor (MHBT) has already demonstrated a large potential for ultra high speed behavior[2,3]. The metallic collector (Schottky contact) is used to reduce both the transit time and the charging time in the base-collector transition layer. Based on a fully self-aligned collector-up process, the entire transistor (except pad connections) is patterned with only one photo-lithographic step using selective wet etching and undercut-based processing.

In this paper we present improvements on the lateral geometry of the device and its consequences on the dynamic behavior. It is shown that the fully self-aligned process allows the fabrication of deep submicron devices (e.g. emitter finger widths smaller than 0.4 mm) without any use of e-beam lithography. As a result, this low-cost process leads to dramatic reduction of the device parasitics. For example the length of the base access region is shorter than 0.2 mm and the base-collector capacitance may be as small as 6 fF. Taking into account these improvements coming from the device processing, MHBTs as fast as fT = fmax = 265 GHz have been fabricated and characterized. This dynamical behavior is analyzed, showing there is still room for even faster behavior.

References:

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# Highly Efficient GaInP/GaAs HBTs for High Power Applications

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## Introduction

GaAs-based heterojunction bipolar transistors (HBTs) are increasingly used for power applications in mobile communications. Beside the huge market of cellular handsets, which requires highly efficient HBTs operated at low supply voltage, the potential of HBTs is very promising for applications in base station circuits, too. This application requires highly linear HBT power cells which can be operated at a collector-emitter voltages around 25V. We report on GaInP/GaAs HBT power cells, which can be operated at bias voltages up to 26V. The dependence of base-collector ($BV_{cbo}$) and collector-emitter ($BV_{ceo}$) breakdown voltages on the collector structure are given. Results of DC characterization confirm the high quality of epi-material and processing. Finally, results of on-wafer power measurements demonstrate good performance.

## Experimental

The high voltage HBT structures (HV-HBTs) are grown on 4-inch GaAs substrates in an Aixtron AIX2400 Planetary™ MOVPE reactor. The layer structures mainly consist of a 700 nm GaAs subcollector layer ($n=5x10^{18}$ $cm^{-3}$), a 2800 nm thick GaAs collector layer (doping variation $n=4 - 20x10^{15}$ $cm^{-3}$), a 100 nm GaAs base layer ($p=4x10^{19}$ $cm^{-3}$), a 40 nm $Ga_{0.51}In_{0.49}P$ emitter layer ($n=5x10^{17}$ $cm^{-3}$), and GaAs and InGaAs contact layers. Si and C are used for the n-type and p-type doping, respectively. The HBT process technology is based on a two-mesa approach in order to access the base and the collector layers. Device isolation is provided by He-ion implantation through the subcollector layer. The lateral emitter and base definition is based on a selective dry-etching process as already described in detail in [1]. $WSiN_x$/Ti/Pt/Au, Pt/Ti/Pt/Au and Ni/Ge/Au/Ni/Au metal systems are used for the emitter, base and collector contacts, respectively. Interconnections are made by Ti/Pt/Au metal and emitter thermal shunts are formed by a 20 µm thick electroplated Au layer [1].

For the etching of the very thick collector layer, which has three times the thickness as compared with the common low-voltage HBTs, sulfuric acid is used taking advantage of its superior selectivity against a 20 nm thin GaInP etch-stop layer. After the collector wet-etching the total topology of the HBT device reaches 4 µm. This very high topology requires optimized processing to deal with. We found that after only slight adaptations our thick-resist stepper-lithography is able to provide the required resolution. A 300 nm thin $SiN_x$ layer served for passivation. The 2 µm thick interconnect metal climbs the base mesa on its gentle sloped side oriented along the (011) plane as shown in Fig. 1.

HBT single finger devices with an emitter area of $3x30$ $\mu m^2$ as well as power cells with a total emitter area of 2400 $\mu m^2$ are fabricated. DC measurements are performed using a commercial wafer mapping system. The power performance is characterized by S-parameter and load-pull measurements at 2 GHz.

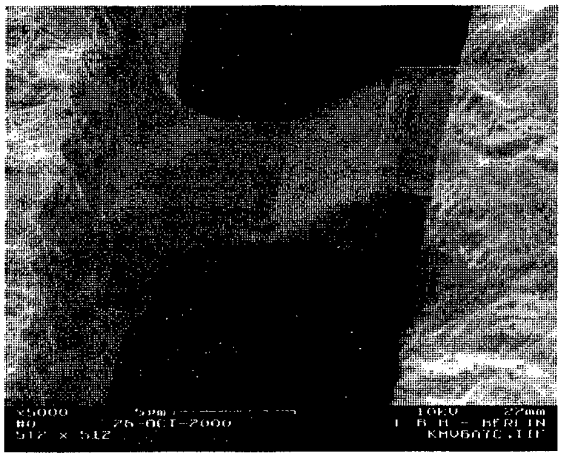

Fig. 1: SEM picture showing the base contact interconnection climbin the 3 µm high base mesa.

## Results

Table 1 shows the measured collector-base ($BV_{cbo}$) and collector-emitter breakdown voltage ($BV_{ceo}$) of HV-HBTs with 2.8 µm collector thickness and different doping levels in comparison with our "standard" low-voltage HBT (collector: 1.0 µm, $2 \times 10^{16}$ $cm^{-3}$). Increasing breakdown voltages with higher collector thickness and with lower doping level are confirmed. High breakdown voltages: $BV_{cbo}$ up to 70 V and $BV_{ceo}$ above 40 V, respectively, are obtained for the lowest collector doping level.

| collector layer | | breakdown voltage | |
|---|---|---|---|
| thickness (µm) | doping ($cm^{-3}$) | $BV_{cbo}$ (V) | $BV_{ceo}$ (V) |
| 1.0 | $2 \times 10^{16}$ | 28 | 13 |
| 2.8 | $2 \times 10^{16}$ | 40 | 18 |
| 2.8 | $8 \times 10^{15}$ | 54 | 26 |
| 2.8 | $6 \times 10^{15}$ | 63 | 33 |
| 2.8 | $4 \times 10^{15}$ | 69 | 41 |

Table 1: Dependence of Collector-base and collector-emitter breakdown voltage on thickness and doping level of collector

Fig. 2 presents typical Gummel plots measured on HV-HBTs and on a "standard" HBT. Comparable high current gain, low recombination currents and good junction idealities are obtained for HV-HBTs. Fig. 3 shows the output characteristics of HV-HBTs with the collector doping of $6x10^{15}$ $cm^{-3}$. At higher current densities ($> 2.5x10^4$ $A/cm^2$) these HV-HBTs are destroyed already at 20V. However, at current densities well below $1x10^4$ $A/cm^2$ device operation at voltages higher than 40 V is possible. The strong dependence of the maximum operating voltage on current density is obviously caused by insufficient thermal stabilization and lack of ballasting of this type of devices.

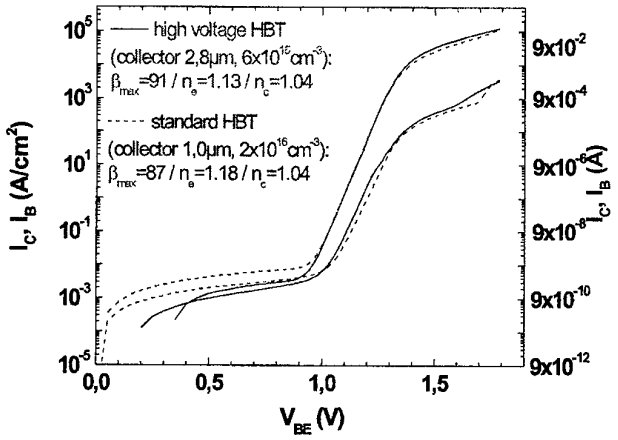


Fig. 2: Comparison of Gummel plots obtained for high voltage HBT and low voltage "standard" HBT (1x3x30 $\mu m^2$).

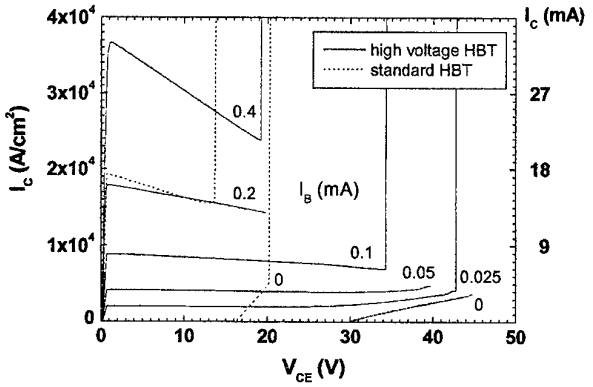


Fig. 3 Output characteristics of high voltage and "standard" HBTs. Destruction of devices is visible after critical $I_c$ and $V_{ce}$ is reached.

S-parameter measurements yield $f_T$ values of 24 GHz and $f_{max}$ values above 50 GHz for 1x3x30 $\mu m^2$ HV-HBTs with a collector doping of $6x10^{15}$ $cm^{-3}$. The onset of Kirk effect is observed if the collector current density exceeds $2x10^4$ $A/cm^2$.

Fig. 4 shows the results of an on-wafer load pull measurements performed on HV-HBTs with different emitter areas. The collector doping was $6x10^{15}$ $cm^{-3}$. The transistors utilized thermal drain structures and emitter ballasting; collector biasing has been 26 V. Before on wafer measurements the wafers have been thinned to 100µm and mounted to a heat sink using thermal grease. According to Fig. 3 a nearly linear scaling of RF output power with total emitter area has been obtained. 2400 $\mu m^2$ devices deliver an output power of 7.5 W at 2 GHz. This corresponds to a power density of about 300 $kW/cm^2$. Typical values for the power added efficiency are around 55%. For these devices the optimum load impedance is in the range of 30 Ω. This high impedance level is a result of the high voltage operation conditions and is more than one order of magnitude higher as compared to low-voltage HBTs of comparable output power. It demonstrates the potential of these power cells to be efficiently combined to very high power microwave amplifiers.

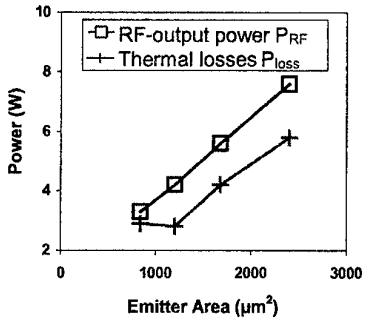


Fig. 4: RF output power P of different power cells versus total emitte area; collector bias: 26 V

## Conclusions

Very promising results are obtained on special HBTs for high-voltage operation. HV-HBTs utilizing thermal drain structures combined with emitter ballasting techniques operated at 26 V and delivered 7.5 W of microwave power at a PAE of 55% at 2 GHz.

## Acknowledgements

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# Design Optimisation of InP/InGaAs HBTs

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Heterojunction Bipolar Transistors (HBTs) based on the InP/InGaAs material system have attracted much attention in recent years. The intrinsic advantages of this system, namely high mobility, small conduction to valence band offset ratio and small band gap of InGaAs among many others, have destined its suitability for a variety of high frequency, low power optoelectronic and telecommunication applications.

In this paper, the design optimisation of InP/InGaAs HBTs for high DC and RF performance is investigated by employing a physics-based analytical model[1]. This model follows the current balancing concept [2, 3], combining both the thermionic-field-emission (TFE) current across the heterointerface at base/emitter (b/e) junction and the diffusion current in the quasi-neutral bulk regions. Appropriate Fermi-Dirac statistics correction is made to the TFE formulation and utilized for all heavy doping layers. Bandgap narrowing (BGN) of heavily doped layers and its effect on the band discontinuity at the b/e heterointerface are also included. Doping dependence of parameters, such as mobility and lifetime, for $In_{0.53}Ga_{0.47}As$ and InP are described by the least square fits to the reported data in the literature. Recombination current in the b/e space charge region, including Shockley-Read-Hall (SRH), radiative and Auger mechanisms are modelled. In addition, at high current levels where the potential drop across the ohmic contacts and the bulk semiconductor region is significant, the actual junction potential is modified by taking into account of the emitter, collector and base resistances due to the ohmic contacts and also the resistivity in the current path. Good agreement is found between the simulation and measurements for the InGaAs/InP HBTs studied.

InP/InGaAs HBTs often incorporate an undoped spacer layer between the base and emitter for the purpose of preventing base dopant out-diffusion and/or lowering the conduction band spike of the b/e heterojunction. Although the insertion of this undoped spacer layer improves the injection efficiency of the device, hence the collector current, the dependency of the base side depletion layer width with the spacer alters the contribution of the SCR from the base side. Figure 1 and 2 show the simulated Gummel plots for typical InGaAs/InP HBTs with low (LB) and high base (HB) doping levels, respectively, for various spacer layer thicknesses. Also shown in Fig. 1 are the measured data for two devices fabricated at King's College London with 20 and 200Å spacer, which agree well with the results predicted by the simulations. It can be seen that for both LB and HB structures, collector current increases with the spacer. This increase is much faster and larger in quantity in the HB than that in the LB structure. For the HB, by insertion of a 60Å spacer layer, the collector current is improved by almost a factor of 300. However, this collector current improvement is accompanied by the base current increase due to the recombination current from the base side. Figure 3 and 4 give the simulated collector current dependence of the DC current gain for the corresponding spacer thicknesses. As it can be seen that, the current gain decreases with the spacer in both cases. For the LB, gain decreases with the initial increase of spacer, but negligible change is seen after 60Å. However, for the HB, the gain reduces only slightly for spacer below 60Å, but decreases significantly and consistently after 60Å to 200Å. It should be noted that this current variation is most apparent at low collector current where recombination is important. These suggest that the spacer has a significant influence on the DC current gain of the InP/InGaAs devices, both in terms of magnitude and its dependency on collector current. Furthermore, depending on the base doping level, the sensitivity of current gain change with respect to spacer layer also differs. For InGaAs/InP HBT structures studied here, due to the recombination current contribution from the InGaAs base, no improvement in gain is made by insertion of the spacer layer. Nevertheless, for HB, since the thin spacer (<60Å) does not reduce the gain much, it can be used to reduce the device turn-on voltage. Details of these results with further theoretical and

experimental DC data will be discussed in the full paper. The basic device structure for simulation is as follows: Emitter: $5x10^{17}cm^{-3}$/1000Å, Base: $1x10^{18}cm^{-3}$ or $1x10^{19}cm^{-3}$/1000Å, Collector: $2.5x10^{16}cm^{-3}$/4000Å.

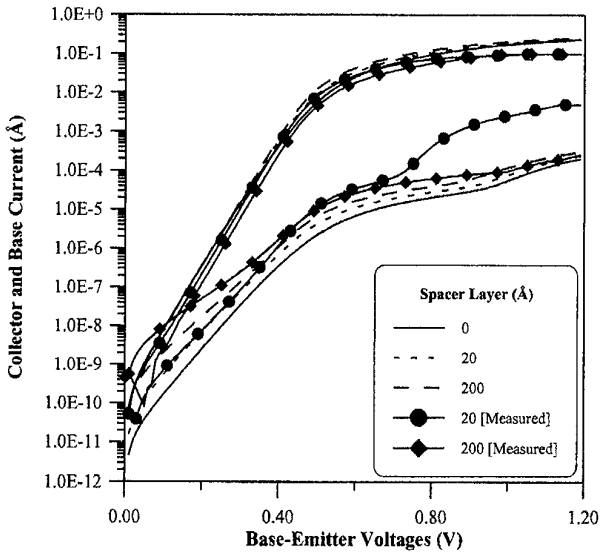


**Figure 1:** Simulated and Measured Gummel Plot of a typical InP/InGaAs HBT with $N_{AB}=1x10^{18}cm^{-3}$ and $W_B$=1000Å

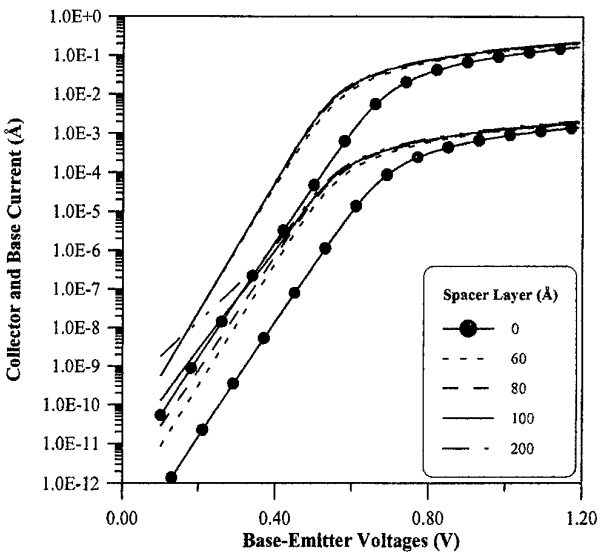


**Figure 2:** Simulated Gummel Plot of a typical InP/InGaAs HBT with $N_{AB}=1x10^{19}cm^{-3}$ and $W_B$=1000Å

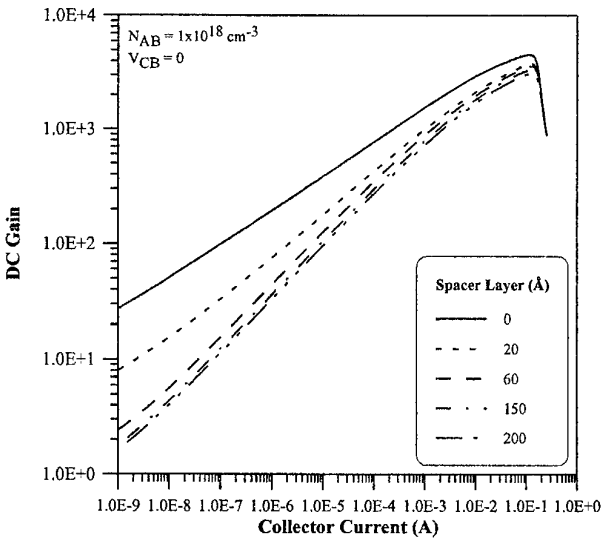


**Figure 3:** Simulated DC current gain of a typical InP/InGaAs HBT with $N_{AB}=1x10^{18}cm^{-3}$ and $W_B$=1000Å

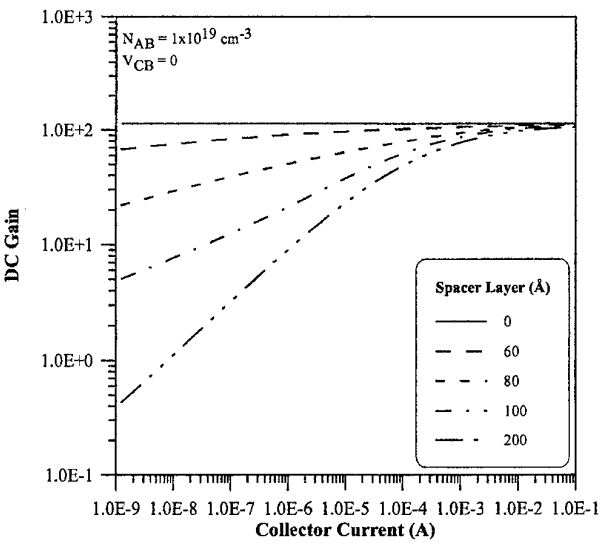


**Figure 4:** Simulated DC current gain of a typical InP/InGaAs HBT with $N_{AB}=1x10^{19}cm^{-3}$ and $W_B$=1000Å

**Acknowledgement:** This project is supported by the UK Engineering and Physical Sciences Research Council.

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## SESSION III
## GaN: material growth and device processing
## Chair: Prof. Vernon David Morgan
## Monday May 28, 2001

| | |
|---|---|
| **2.30 pm**<br><br>**INVITED** | **AlGaN/GaN HEMT's: epitaxial growth issues on various substrates, devices fabrication, and insertion of GaN component into circuits.**<br>*Joseph Smart*<br>V.P. of advanced Technology,RF Nitro Communications |
| **2.55 pm** | **Organometallic Vapor Phase Epitaxy Growth and Optimization of AlN/GaN MIS-type Heterostructures**<br>*S.M. Hubbard, D. Pavlidis, V. Valiaev, A. Eisenbach*<br>Department of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor, MI 48109-2122, USAD. |
| **3.10 pm** | **InGaN - a material for electronic devices?!**<br>*M. Seyboth[(a)], C. Kirchner[(a)], M. Kamp[(a,b)], I. Daumiller[(c)], M. Neuburger[(c)], E. Kohn[(c)]*<br>(a) Dept. of Optoelectronics, University of Ulm, D-89081 Ulm, Germany<br>(b) now with Global Light Industries, 47475 Kamp-Lintfort, Germany<br>(c) Dept. of Electron Devices and Circuits, University of Ulm, D-89081 Ulm,Germany |
| **3.25 pm** | **Power and Frequency Limits of AlGaN/GaN HEMT's**<br>*L. F. Eastman,*<br>Electrical and Computer Engineering Cornell University, Ithaca, NY 14853-5401 |
| **3.40 pm** | **Quantum 1/f Noise in GaN/AlGaN HFETs and Phase Noise in RTDs**<br>*P. H. Handel*<br>Department of Physics and Astronomy, Univ. of Missouri-St. Louis,St. Louis MO 63121 |
| **3.55 pm** | **Fabrication of 0.5-μm-AlGaN/GaN HEMTs based on a 2-inch-Stepper-Process**<br>*J. Hilsenbeck[(a)], R. Lossy[(a)], J. Würfl[(a)] and H. Obloh[(b)]*<br>(a) Ferdinand-Braun-Institut für Höchstfrequenztechnik, Albert-Einstein-Straße 11, 12489 Berlin, Germany<br>(b) Fraunhofer-Institut für Angewandte Festkörperphysik, Tulla-Straße 72, 79108 Freiburg, Germany |

# AlGaN/GaN High Power Transistor Materials and Devices

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Over the past several years, rapid advances have been demonstrated in epitaxial growth and device processing of GaN-based transistors. As the technology matures, substrate selection, device fabrication techniques, and reliability become important factors in the commercialization of GaN. Undoped AlGaN/GaN transistor structures have been grown on sapphire, SiC, and silicon substrates. Discrete GaN-based devices have been fabricated from all three of these substrates and compared. The best microwave performance is observed on device on SiC substrates, followed by sapphire, then silicon.

## Introduction

The synthesis of GaN and related alloys is accomplished by flow modulation techniques in a custom-built, cold wall OMVPE reactor. A unique high temperature nucleation process using thin AlGaN films is used to produce atomically flat growth on sapphire, SiC, and silicon substrates. This process simplifies the growth by eliminating large temperature ramps, while producing high resistivity (>1 x$10^8$ Ω–cm) GaN films. An additional AlN barrier layer is inserted just after planarization of the film on SiC and silicon substrated structures to reduce affects from the substrates. Undoped AlGaN/GaN heterostructures were grown on c-plane sapphire, 4H semi-insulating SiC, and 10 Ω-cm (111) p-type silicon.

Devices were fabricated using standard photolithography and e-beam techniques. Ohmic contacts were formed using a Ti/Al/Ti/Au metallization. Ni/Au was used for the Schottky gates. In all cases silicon nitride was used for surface passivation of the ungated regions. Devices were dc and RF tested and compared. In addition, channel temperatures were measured on large periphery devices fabricated on sapphire and SiC substrates.

## Results and Discussions

Nucleation conditions varied substantially between the three different substrates. After optimization of the Al content in the AlGaN nucleation layer, atomically flat device quality GaN films were achieved on each substrate type. The resulting 2DEG at the AlGaN/GaN heterostructure exhibited room temperature mobilities of 1700 $cm^2/V{\cdot}s$, 1505 $cm^2/V{\cdot}s$, and 900 $cm^2/V{\cdot}s$ on sapphire, SiC, and silicon respectively, all with a nominal 1 x $10^{13}$ $cm^{-2}$ electron sheet density. The mobility on SiC is limited by defects that originate in the substrate and propagate through the entire epitaxial layer. Although the heterostructure on silicon substrates is atomically flat as determined by TEM studies (Figure 1), the relatively low mobility on silicon is attributed to scattering from regions were the crystal is tilted by 0.25 ° relative to the <0001> direction. This tilt originates

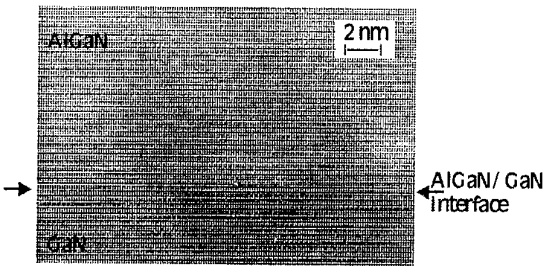


Figure 1. High resolution TEM of AlGaN/GaN heterostructure on a silicon substrate. Arrows indicate the heterostructure showing an atomically abrupt interface

from defective regions in the nucleation layer unique to growth on silicon. Other complications with GaN epitaxial growth on silicon include surface conversion from p-type or semi-insulating to n-type when heated in hydrogen, and auto-doping of the GaN buffer layer near the substrate/epitaxy interface.

A small-signal comparison of transistors fabricated from the different substrates is shown in Figure 2. The small-signal unity current gain ($f_t$) was measured at the peak extrinsic transconductance of 300, 215, and 150 mS/mm for SiC, sapphire, and silicon substrated devices. The lower than expected values for devices on silicon is a direct result of the conductive substrate charge being coupled under small-signal conditions.

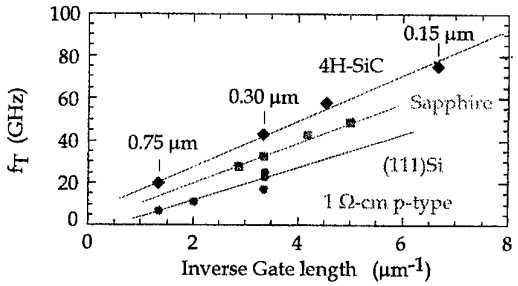


Figure 2. Measured extrinsic $f_t$ versus inverse gate length for AlGaN/GaN HEMTs

Removing the silicon substrate under the active regions improves the frequency response of the transistors, indicating that ac coupling to the substrate is the limiting factor for these transistors. However, by releasing the GaN epitaxy from the silicon substrate effectively removes the heat-sinking path for heat dissipated by the device. Novel heat sinking techniques will have to be developed before GaN on silicon becomes a commercially viable technology.

## Conclusions

Device quality GaN films have successfully been grown on sapphire, SiC, and silicon substrates. High room temperature electron mobilities at high sheet densities have been achieved on heterostructures grown on each substrate type, translating into low channel resistivity adequate for transistor applications. Devices fabricated on silicon substrates exhibit lower than expected frequency response, and complicate the growth process.

# Organometallic Vapor Phase Epitaxy Growth and Optimization of AlN/GaN MIS-type Heterostructures

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III-Nitride based MODFET devices have shown great promise for high-frequency/high-power applications. For the most part, these devices are based on AlGaN/GaN type heterostructures. The binary compound AlN is also expected to be a good insulating material with high dielectric constant. There exists the possibility of using an AlN/GaN system to create metal-insulator-semiconductor field effect transistors (MISFETs) [1]. Use of an AlN insulator has the advantage of maintaining high electron mobility in the channel and at the same time improving transconductance without degradation of gate leakage [2]. Unfortunately, there exists a large lattice mismatch between AlN and GaN. From the growth standpoint, we are challenged to grow both high quality AlN and GaN epilayers, which also exhibit good electronic properties.

Low-pressure Organometallic Vapor Phase Epitaxity (OMVPE) was used to grow AlN/GaN MIS-type heterostructures. Grazing Incidence X-Ray Reflectivity (GIXRR) was used to calibrate the AlN growth. In addition, X-Ray Diffraction and Atomic Force Microscopy were used to verify GaN and AlN material quality and surface morphology. Experiments were conducted by varying both the AlN thickness (from 30 Å to 350 Å) and the AlN V/III ratio (from 1.25 slm $NH_3$ to 5 slm $NH_3$).

For the highest V/III ratio, AFM scans show the AlN is growing in a 3-D island growth mode often seen for III-nitride materials with high Al composition. Surfaces of these samples exhibit defects 100-200 nm in size propagating out from dislocations in the underlying GaN channel layer. As seen in Figure1, these defects decrease in size and density for very thin AlN layers, indicating the presence of an initial AlN wetting layer before the formation of defects [3].

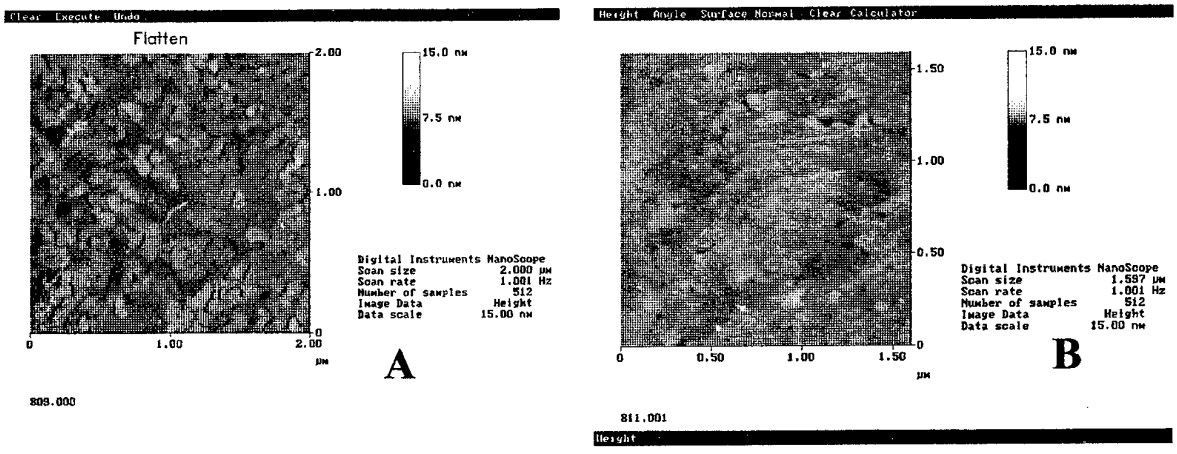


***Figure 1. (A) AFM scan of 8 nm thick AlN layer showing typical defect formation (B) AFM scan of 5nm thick AlN showing reduction of defects for thin AlN layers.***

Van der Pauw Hall-effect measurements were performed on the high V/III ratio samples at temperatures ranging from 20K to 300K. As the AlN thickness was increased, 2DEG sheet carrier concentration increased and Hall mobility decreased. The decrease in electron mobility with increasing AlN thickness is related to a higher percent of the sheet carrier concentration being located very near the interface for thicker AlN [4]. Interface scattering is thus increased and mobility degraded. The optimal AlN thickness was found to be approximately 50 Å. The measured room temperature and 20K mobilities for this sample were 980 $cm^2/Vs$ ($n_s$=8.14 x $10^{12}$ $cm^{-2}$) and 3230 $cm^2/Vs$ ($n_s$=7.76 x $10^{12}$ $cm^{-2}$), respectively. To our knowledge, this is the best reported mobility for OMVPE grown AlN/GaN MIS structures.

In addition, the effect of V/III ratio on AlN surface morphology was studied. The V/III ratio was varied by changing the ammonia flow during AlN growth. GIXRR was again used to calibrate the AlN thickness as a function of V/III ratio. Three 11 nm thick AlN samples of varying ammonia flow (1.25 slm, 2.5 slm, and 5 slm) were studied using AFM and Hall effect measurements. Defect formation was drastically reduced in the case of 1.25 slm and 2.5 slm ammonia flow (see Figure 2b). In Figure 2a we see the effect of the V/III ratio on the electronic properties of the structures. The optimal ammonia flow in terms of mobility and sheet carrier concentration was found to be 2.5 slm ($\mu$ = 891 $cm^2/Vs$, $n_s$ = 2.15e13 $cm^{-2}$). Further work to optimize the AlN thickness at this V/III ratio is in progress.

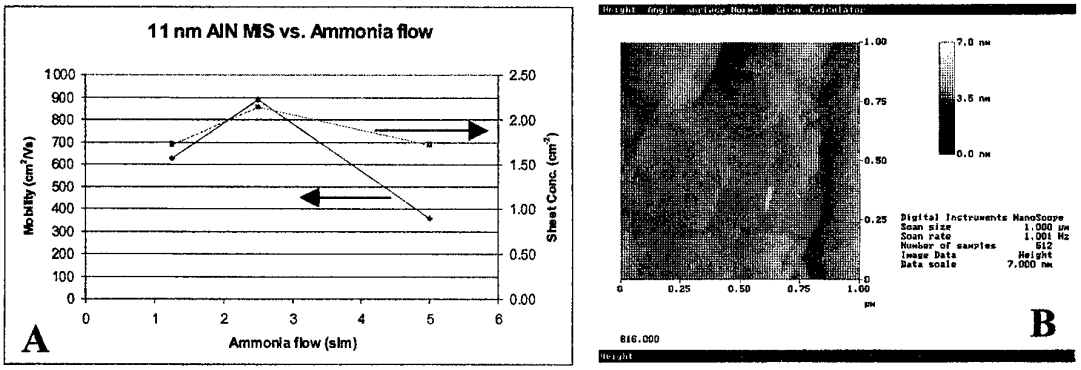


***Figure 2. (A) Hall properties of 11nm AlN MIS structures vs. V/III ratio (B) AFM scan of 11 nm AlN structure grown with 1.25 slm ammonia flow.***

## Acknowledgments

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# InGaN – a material for electronic devices?!

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## Introduction

**AlGaN/GaN heterostructure** field effect transistors have demonstrated **highest microwave power densities** and high efficiencies due to the materials high breakdown field, high channel sheet charge density and 2DEG properties [1]. III-nitrides are highly polar materials generating image charges of the bonded polarization charges in the lattice on the surfaces. These image charges are dipole charges positioned at opposite planes, namely for AlGaN/GaN FET structures at the substrate/GaN backplane, the AlGaN/GaN interface and at the surface of the AlGaN layer. The surface however is a most sensitive portion of any planar device and such **surface image charges** could be identified as a source of the large signal RF **current compression** in a number of GaN-based HFETs [2].
In case of an **InGaN channel** sandwiched in between two GaN layers, both parts of the image charge dipole are located within the quantum well. For Ga-face material at the GaN surface the spontaneous polarization image charge is positive as in the AlGaN/GaN case. At 10% In-content the difference between the spontaneous polarization of the GaN and InGaN lattice contributes to only 10% to the interface charges. 90% is generated by the piezo polarization due to the strain in the InGaN layer. However, since both dipole charges reside in the quantum well, the FET channel is ambipolar. Biasing the structure like in the case of an n-type FET, the source region may become n-type under certain conditions and the drain p-type, thus developing a pn-junction in between. To obtain an n-type channel alone, the hole concentration needs to be compensated by a shallow donor. The compensation can be accommodated by channel doping of the lower part of the InGaN well or through modulation doping from a doping spike in the bottom GaN barrier layer. Therefore in GaN/InGaN/GaN HFETs the image polarization channel charge is not mirrored at the surface. During modulation of the channel by the gate, the channel charge dipole is in essence that of the 2DEG and the donor, responding to the signal with the time constant of the dielectric relaxation. It is therefore expected that these devices show an essentially reduced large signal RF current compression phenomena.

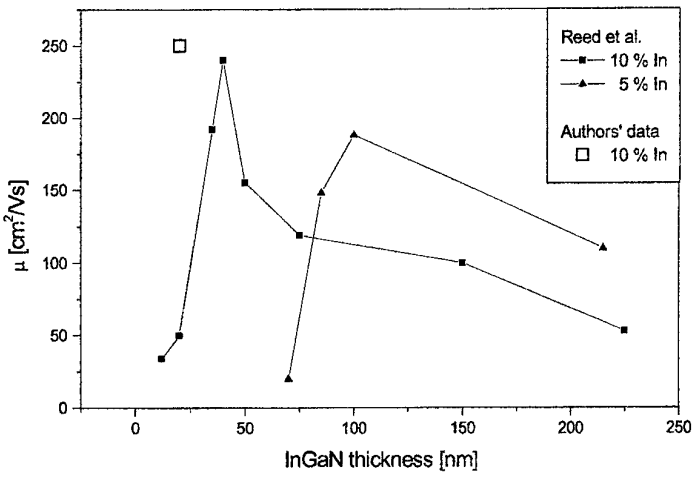


**Figure 1** Electron mobility of GaN/InGaN/GaN heterostructures with various In content and InGaN layer thickness.

## Growth and Properties of InGaN

**Growth** of the device structures was performed in an Aixtron AIX 200 RF horizontal reactor system. On sapphire substrate a nucleation layer was deposited, followed by a 3 μm thick GaN buffer, grown at 1050°C.

The **device structure** consists of a 20 nm InGaN channel, grown at 800 °C, using TMGa and TMIn as metalorganic sources and is capped by a 20 nm GaN layer. Carrier gas for InGaN growth is nitrogen. N-doping with silan as source is either realized in the GaN below or in the first 10 nm of the channel. For device performance, a doping profile with steep ramps and a well defined total charge is necessary.
As InGaN is mostly employed as active layer in **optoelectronics devices**, optimization of InGaN layers is usually done in terms of photoluminescence and electroluminescence efficiency. Typical QW structures consist of 2 - 3 nm thick InGaN wells in between GaN layers, often it is strived for quantum dot formation to increase the recombination efficiency. Requirements for horizontal **electronic devices** are quite different: a 20 nm thick InGaN layer serves as channel, therefore the indium content had to be reduced approximately 10 % to obtain reasonable horizontal mobilities.
Fig. 4 shows a comparison of **mobilities** for 20 nm channel thickness in comparison to Reed et al. [3]. This study on critical layer thickness determination yielded a maximum mobility of $\mu$=240 cm$^2$/Vs for a indium content of 10 %. The overall agreement with our data ($\mu$=250 cm$^2$/Vs for 10 % In) indicates a typical range for mobilities for InGaN quantum wells optimized for optical properties. Thus, further InGaN–growth studies oriented versus improved horizontal electrical properties may lead to a considerably enhanced device performance.

## Device Characteristics

Fig 2. shows the device characteristics of a **channel doped FET device** with an In-content of 7% in the InGaN well (as measured by photoluminescence on the control sample). For hole dipole charge compensation the rear 10 nm of the channel were doped by Si to nominally 2x10$^{18}$ cm$^{-3}$. The device can be pinched off with a gate bias of $V_g$=-2.0 V and no parallel path is observed related to over-compensation.

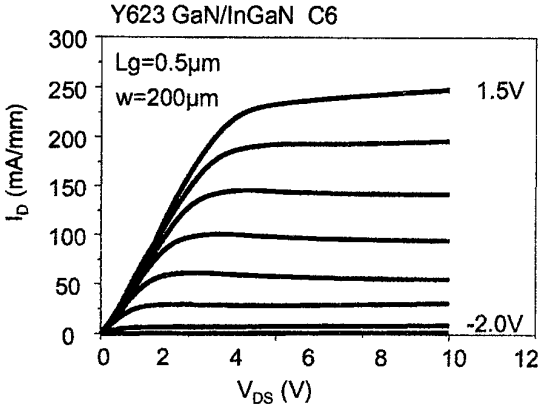


**Figure 2.** Output characteristics of a GaN/InGaN/GaN FET with channel doping for hole compensation with an estimated 7% In-content.

In agreement with the Schottky diode characteristics for high voltage characteristics a **maximum drain bias above 100 V** could be applied. Placing an optimum load line across this characteristic a maximum **RF-power capability of 2.5 W/mm** could be inferred from this experimental structure
Since the prime motivation for this work was the reduction in large signal RF current compression, the large signal characteristics were tested as described in [5]. Using a 50 Ω load, the input of the device was adjusted to obtain the maximum output current swing. The measurement is performed using three different setups and multiple calibrations
The maximum frequency was determined by role off in gain, which could not be compensated by the input signal above 6 GHz ($f_T$ = 9 GHz). Within the measurement precision **no current compression** in class A operation was observed.

### Literature


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# Power and Frequency Limits of AlGaN/GaN HEMT's

By

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GaN has a large band gap (3.4 V), which allows electrical field strength up to 3 x $10^6$V/cm before avalanche breakdown. This allows up to 7.5 times as high a drain-source voltage as for GaAs-based microwave field effect transistors. The current can also be raised by the same ratio, to maintain the same optimized load impedance, yielding up to 56 times as much power into this same load impedance. In order to reach the higher current value, the periphery of the GaN HEMT is made larger. The frequency response is presently nearly similar to that of GaAs HEMT's, due to a similar value of the electron transit velocity. Using semi-insulating SiC substrates, which have about 7.5 times the thermal conductivity of GaAs, the normalized heat power dissipated can be at least 7.5 times that of GaAs.

Typically a 200-300 Å $Al_{.3}Ga_{.7}N$ barrier is grown on the Ga-face of ~ 1 μm thick semi-insulating epitaxial GaN buffer layer, which in turn is on AlGaN nucleation and sub-buffer layer on the SiC substrate. Either 1040°C OMVPE, or 800°C gas-source MBE can be used. The structure is entirely undoped, relying on the difference in electrical polarization at the top heterojunction to induce the ~ 1 x $10^{13}$/cm$^2$ 2DEG. A shallow ECR $Cl_2$ etch is used to isolate the HEMT mesas, and Ti/Al/Ti/Au, annealed at 800° C for 30-40 sec, forms the ohmic contact. The Ni/Au Schottky gate is formed with a mushroom-shaped cross section, using an exposed multi-layered electron beam resist. A $Si_3N_4$ passivation layer is deposited and air bridges are added for inter connections. The drain-source breakdown voltage and the reciprocal of the cut off frequency both vary linearly with the effective gate length, made up of the gate footprint plus twice the barrier thickness. For .20 μm effective gate length, these values are 35 V and 74 GHz, respectively.

In addition to the breakdown voltage limit, there is a limit imposed by self- heating, lowering the expected efficiency and power. The reciprocal of the low field mobility experimentally rises as $(T/300)^{1.8}$, raising the knee voltage due to the self-heating. Thermal simulations show that the normalized temperature rise of the channels, placed 50 μm apart, is ~

12°/W for large periphery HEMT's, but is only 6.5 °/W for a two-channel .25 mm periphery HEMT. The temperature rises super-linearly due to the SiC reduced thermal conductivity at elevated temperature. At 10 W/mm heat dissipation, the small periphery HEMT knee voltage more than doubles, lowering the drain efficiency. In class B operation at 10 GHz, with two .3 μm gates, separated by 50 μm, the .25 mm periphery HEMT has 65% power-added efficiency when biased at 13-15 V, but this becomes 42% power-added efficiency when biased at 45-48 V. Automatic tuning is used on both the input and the output of the HEMT, and 7.6 W/mm is the output normalized power at the higher drain bias, leaving 10 W/mm heat dissipation.

The frequency response is only moderately affected by the rise in channel temperature. Monte Carlo calculations have shown that the peak electron velocity reduces only 5% for 100° temperature rise. At room temperature the average transit velocity is $\leq 1.3 \times 10^7$ cm/s. Monte Carlo calculations for electron transport in bulk GaN show peak electron velocity of $\sim 2.85 \times 10^7$ cm/s at room temperature, a value close to the experimental value determined from femto-second optical pulse-probe measurements. In the HEMT technologies based on GaAs and InP substrates, the average transit velocity derived from cut off frequency, has been 80-85% of the peak velocity value. With improved design, and technology of materials and processing, the average transit velocity of electrons in GaN HEMT's should reach $2.0 - 2.4\ 10^7$ cm/s, approaching the value gotten in InP HEMT's.

In conclusion, AlGaN/GN HEMT's will dominate in microwave and mm wave high power amplifiers in the future, opening up a new technology for Radar and communication transmitters.

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# Quantum 1/f Noise in GaN/AlGaN HFETs and Phase Noise in RTDs

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**Abstract** -- The present paper applies the quantum theory of 1/f noise to predict the 1/f fluctuations in GaN/$Al_{0.15}Ga_{0.85}N$ doped-channel HFETs. It compares the experimentally measured values of the effective 1/f noise parameter with the theoretical value, as a function of the device parameters, of drain voltage, drain current and gate voltage. There is remarkable agreement between theory and experiment, as demonstrated by the dependence of the noise on gate voltage. The quantum 1/f theory is also used to calculate from first principles the 1/f noise present in the device parameters and in the resulting system frequency from resonant tunneling diodes (RTDs). In general, quantum 1/f fluctuations in the dissipative elements lead to a $Q^{-4}$ dependence of the spectral density of phase noise, where Q is the quality factor.

**I. HFETs.** To find the noise, the number of charge carriers is first taken as the net induced charge, divided by the charge of the electron. The element of resistance dR along the current can be written

$$dR = dy/q\mu N' = \frac{dy}{Z\mu_n C[V_{GS}-V_T-V(y)]} \quad , \tag{1}$$

where $\mu_n$ is the electron mobility, N' the number of carriers per unit length of the channel, C the gate capacity per unit area, $V_{GS}=V_G-V_S$ the gate to source voltage, $V_T$ the threshold value of $V_{GS}$, and V(y) the potential the channel at a distance y from the source, or Y-v from the drain. Note that the rectangular bracket in the denominator is a first approximation only, based on the simple capacitor model. In general, as we shall see below, Fermi statistics is applicable, essentially replacing the bracket [ ] by $k_BT\{\exp([\,]/k_BT) -1\}$, where $k_B$ is Boltzmann's constant. The quantum 1/f noise in the element of resistance is given by the basic quantum 1/f formula for mobility fluctuations [2]

$$\frac{<(\delta dR)^2>_f}{(dR)^2} = \frac{\alpha_o}{fdN} \quad \text{with} \quad \alpha_o \equiv (2\alpha/\pi)[(1/1+s)(2(\Delta v/c)^2/3 + (s/1+s)]; \; s\equiv 2N'e^2/m_ec^2; \; \alpha\equiv e^2/c\hbar \tag{2}$$

Here $\alpha$ is the fine structure constant 1/137, dN is the number of carriers in the element of resistance

$$dN = ZQ_n dy/q \tag{3}$$

and $Q_n=-C(V_{GS}-V_T)$ is the charge per unit area under the gate, while q=-e is the charge of the electron and $m_e$ the electron mass. Using Eq. (1) for dR, and Eq. (3) for dN, we obtain

$$f<(\delta dR)^2>_f = [dy/q\mu N']^2\frac{\alpha_o}{fdN} = -\frac{q\alpha_o dy}{\mu_n^2 Z^3 C^3[V_{GS}-V_T-V(y)]^3} \; . \tag{4}$$

Multiplying on both sides with the channel current

$$I = -dV/dR = -Z\mu_n C[V_{GS}-V_T-V(y)]dV/dy \tag{5}$$

and integration, yields

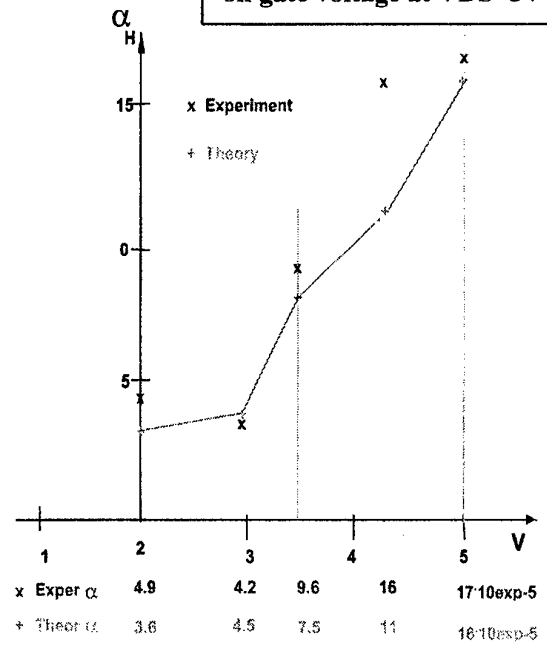
$$fI<(\delta R)^2>_f = \int_0^{V_{DS}} \frac{q\alpha_o dV}{\mu_n Z^2C^2[V_{GS}-V_T-V]^2} = \frac{q\alpha_o}{\mu_n Z^2C^2}\frac{V_{DS}}{V_G^*(V_G^*-V_{DS})} \; . \tag{6}$$

Here $V_G^*=V_{GS}-V_T$. This simple summation of spectra is justified, because both theory and experiment have shown that the fluctuations of the various elements dR are uncorrelated, down to the smallest experimentally accessible lengths, and down to the electronic correlation length. Dividing both sides with $IR^2$ and replacing $V_{DS}/I$ by R on the r.h.s., we obtain with Fermi statistics as mentioned above

$$fI_{Ch}<(\delta R)^2>_f = \int_0^{V_{sat}} \frac{\alpha_{coh}dV}{q\mu N'^2} + \int_{V_{sat}}^{V_{DS}} \frac{\alpha_{conv}qv_s^2 dV}{q\mu I_{Ch}^2} \approx \frac{\sqrt{2}}{q\mu}\int_0^{V_{DS}} \frac{\alpha_H(N')dV}{I_{Ch}^2/q^2v_s^2 + Z^2D_{eff}^2V_{th}\ln\{1+\exp[(V_G^*-V)/V_{th})]\}} \; . \tag{7}$$

Here we used the conventional quantum 1/f noise formula for the sub-threshold part of the channel. For a GaN/$Al_xGa_{1-x}N$ doped n-channel HFET this yields the spectral density of $V_{DS}$ in terms of device width Z, current $I_{Ch}$, and thermal voltage kT/q by renewed multiplication with $I_{Ch}$.

**Fig. 1: Dependence of $\alpha_H$ on gate voltage at VDS=5V**




Using the fact that the velocity of the carriers shows strong saturation in that section, to include impact ionization effect, we split up the integral at V(y) = $V_{G*}$-$V_{th}$ and write the corresponding second part of the integral in Eq. (20) separately, with the number of carriers per unit channel length defined as N' = $I_{ch}/qv_s$, where $v_s$ is the saturation velocity. We also replace the ratio v(E)/E by 3.5 $\mu_0$, where $\mu_o$ is the low-field mobility. This allows us to find a theoretical expression for the experimental 1/f noise constant defined by

$$\alpha_{exp} \equiv [S_V/V^2]\, L^2/Re\mu = \qquad (8)$$

$$\frac{I_{ch}L^2}{qV_{DS}^2\mu^2}\{\frac{\alpha_H^{coh} I_{ch}}{qZ^2D_{eff}^2 V_{th}V_{DS}} + \frac{\alpha_H^{conv} qv_s^2}{I_{ch}}(1-\frac{V_G^*}{V_{DS}}+\frac{V_{th}}{V_{DS}})\}$$

R is the channel resistance and $V_G^*=V_{GS}-V_T$. The experimental values of $\alpha$ measured by Balandin et al. [1], are 4.9, 4.2, 11, 16 and 17, in units of $10^{-5}$ corresponding to $V_G^*$ values of 2, 3, 3.45, 4.25 and 5 volts respectively. Eq. (3) yields about 3.6, 4.5, 7.5,11 and 16 in the same units. The agreement between theory and experiment is remarkable, (Fig. 1) considering the absence of free parameters in this first principles quantum 1/f calculation.

**II RTDs.** Resonant tunneling diodes have been proposed as generators of THz oscillations and radiation. They consist of two potential barriers enclosing a quantum well. Electrons penetrating the potential barriers by tunneling are controlled by the quasistationary energy levels defined by the penetrating the potential barriers by tunneling are controlled by the quasistationary energy levels defined by the potential well. If their energy is close to the first energy level in the well, resonance occurs, and a peak $I_P$ of the current through the diode occurs. This corresponds to an applied bias voltage $V_P$. If, however, the applied voltage increases further, only a negligibly small non-resonant current trickle remains at the voltage $V=V_V$ and a broad valley is observed in the I/V characteristic. Scattering processes that reduce the energy of the carriers to a value close to $eV_P$ will always be present, generating a finite current minimum $I_V$ at $V_V$. Between $V_P$ and $V_V$ there is a negative differential conductance

$$G=-(I_P-I_V)/(V_V-V_P) \qquad (9)$$

on the I/V curve, that is used to generate oscillations. The 1/f noise in $I_V$ is given by Eq. (2) with

$$(\Delta v/c)^2=2eV_V/m. \qquad (10)$$

Taking for instance $V_P$=0.4 V, $I_P$=2.5 $10^8$A/m$^2$, $V_V$=0.6 V, $I_V$=4 $10^7$ A/m$^2$, we obtain with $m_{eff}$=0.068 $m_o$,

$$NI_V^{-2}S_{I_V}(f) =2\alpha A/f=7.4/0.068\ 10^{-9}=1.3\ 10^{-7} \qquad (11)$$

N is given by

$$N=\tau I_V/e, \qquad (12)$$

where $\tau$ is the life time of the carriers. With a cross-sectional area of $10^{-6}$ cm$^2$ and $\tau=10^{-10}$, we obtain N= 2.5 $10^6$.
Finally, the quantum 1/f frequency fluctuations can be obtained from the formula [2]

$$S_{\delta\omega/\omega}=(1/4Q^4)S_{\delta G/G} \qquad (13)$$

This finally yields with Eq. (2), both for $S_{\delta\omega/\omega}$ and for the spectral density $S_{\delta\phi/\phi}$ of phase fluctuations

$$S_{\delta\omega/\omega}=(1/4Q^4)(4\alpha/3\pi)(2eV_V/mc^2) \equiv (f/2\pi\nu)^2 S_{\Delta\phi}, \qquad (14)$$

for the fractional frequency fluctuation spectrum exhibited by the RTD if included in an RF circuit of quality factor Q.

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# Fabrication of 0.5-μm-AlGaN/GaN HEMTs based on a 2-inch-Stepper-Process

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We report on DC parameters and radio frequency small signal performance of AlGaN/GaN-HEMTs based on a 2-inch process line using stepper lithography.

The epilayers were grown by MOCVD on sapphire and consist of a 2.8 μm semi insulating GaN buffer layer, a 3 nm AlGaN spacer layer, a 12 nm doped AlGaN supply layer ($N_D$ = 1x10$^{19}$ cm$^{-3}$), a 10 nm AlGaN barrier layer and a 5 nm thin GaN cap layer.

The HEMT fabrication starts with the ohmic contact (Ti/Al/Ti/Au/WSiN). Since the WSiN metallization layer is done by a sputter process, the e-beam-evaporated Ti/Al/Ti/Au-layers are totally encapsulated. Thus the contact morphology is still smooth with excellent contact edges even after annealing at 850°C. The average value of the ohmic contact resistance is 0.54 Ωmm. After the contact fabrication device isolation by mesa etching has been done, followed by the gate contact ($L_G$ = 0.5 μm), the interconnection metallization and the air bridge technology. Figure 1 shows SEM pictures of an AlGaN/GaN HEMT.

From DC measurements excellent homogeneity could be observed. Within a range of 2 - 3 % the average values of the maximum transconductance $g_{m,max}$, the maximum drain-source-current $I_{DS,max}$ and the pinch off voltage $V_P$ are 205 mS/mm, 620 mA/mm and -3.95 V, respectively (Figure 2).

The average value of the source resistance $R_S$ determined from DC measurements is 1.04 Ωmm leading to an intrinsic transconductance of 275 mS/mm. With a gate-2DEG-separation of 35 nm the effective 2DEG electron velocity is calculated to be 1.1x10$^7$ cm/s, which is one of the best values ever reported. Together with the Hall measurements ($n_{2DEG}$ = 9x10$^{13}$ cm$^{-2}$, $\mu_n$ = 900 cm$^2$/Vs, T = 300 K) these data suggest excellent microwave performance.

From small signal equivalent circuit extraction a very good correspondance between theory and measurement could be observed (see Figure 3 a). The extracted source resistance is 1.1 Ωmm, thus the intrinsic transconductance is determined to be 263 mS/mm and agrees very well with the DC data. With a gate length of 0.5 μm cut off frequency $f_T$ and the maximum frequency of oscillation $f_{max}$ are 23 and 60 GHz, respectively ( see Figure 3 b).

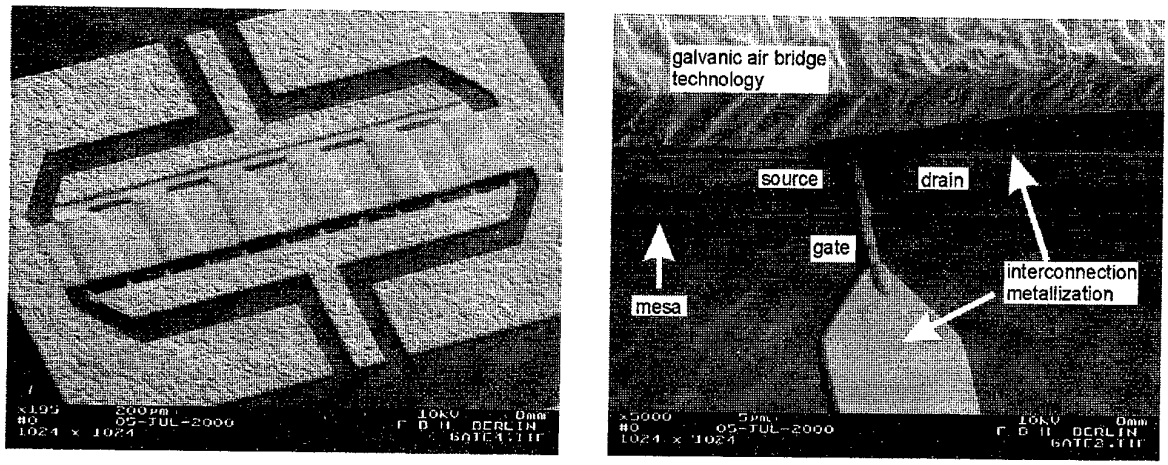
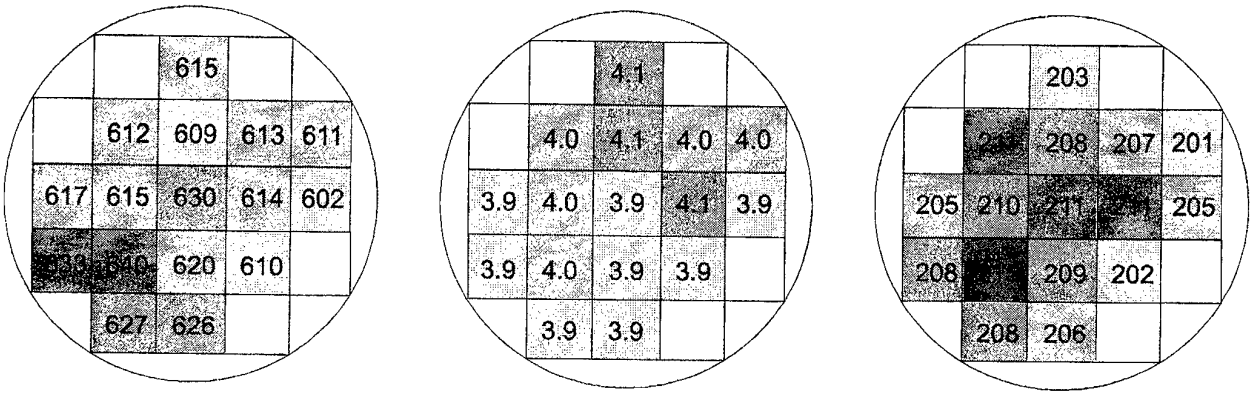



Figure 1: SEM image of an AlGaN/GaN-HEMT utilizing air bridge technology. Left: AlGaN/GaN multi finger Transistor, right: AlgaN/GaN HEMT in detail.




$I_{DS0}$ = 616 mA/mm, σ = 11 mA/mm

$I_{DS0}$ = 3.95 V, σ = 0.08 V

$g_{m,max}$ = 206 mS/mm, σ = 4 mS/mm

Figure 2: DC-wafer maps of saturation current at 0V gate bias $I_{DS0}$, Pinch-off voltage $V_p$ and extrinsic transconductance $g_{m,max}$. The main flat is located at the top of the wafer maps.

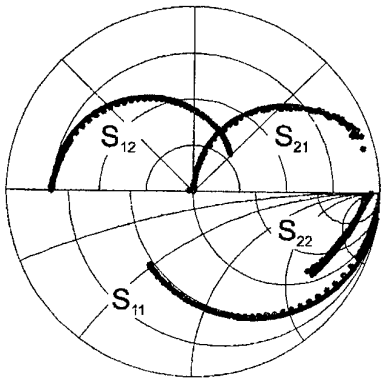



Figure 3 a: Hybrid chart of measured and simulated S-parameters ($V_{GS}$ = -2.5 V, $V_{DS}$ = 12 V, f = 50 MHz .. 50 GHz).

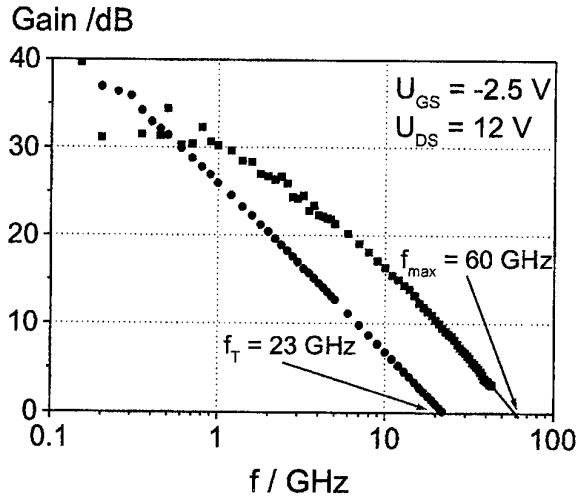



Figure 3 b: Current gain and maximum unilateral gain ($V_{GS}$ = -2.5 V, $V_{DS}$ = 12 V, f = 50 MHz .. 50 GHz).

# SESSION IV
# Characterization of GaAs and InP-based devices
# Chair: Prof. Werner Baechtold
# Monday May 28, 2001

| | |
|---|---|
| **4.40 pm**<br><br>**INVITED** | **Design and Fabrication Technology of Gate and Gate Recess for Ultrahigh-Speed InP-Based HEMTs**<br>*T. Suemitsu*[1], *T. Ishii*[1] *and H. Yokoyama*[2]<br>(1) NTT Photonics Laboratories 3-1 Morinosato Wakamiya, Atsugi, Kanagawa 243-0198, Japan<br>(2) NTT Advanced Technology Corp. 3-1 Morinosato Wakamiya, Atsugi, Kanagawa 243-0198, Japan |
| **5.05 pm** | **Fast Traps in InAlAs/InGaAs/InAlAs/InP 2-DEG Channels**<br>*A. Matulionis*[a], *V. Aninkevičius*[a], *L. Ardaravičius*[a], *J. Liberis*[a], *and D. Gasquet*[b]<br>(a) Semiconductor Physics Institute, A. Goštauto 11, 2600, Vilnius, Lithuania<br>(b) CEM2, Université Montpellier II, Place E. Bataillon, F-34095 Montpellier, France |
| **5.20 pm** | **Evaluation of SiNx Passivation on InP HEMTs at Room and Cryogenic Temperature**<br>*R. Limacher, M. Rudin, O.J. Homan, W. Bächtold*<br>Institut für Feldtheorie und HöchstfrequenztechnikEidgenössische Technische Hochschule Zürich, CH-8092 Zürich, Schweiz |
| **5.35 pm** | **Simulation of ultra short channel InAlAs/InGaAs/InP High Electron Mobility Transistors by a Coupled Solution of the Schrödinger Equation with a Hydrodynamic Transport Model**<br>*J. Höntschel*[a], *R. Stenzel*[a], *W. Klix*[b], *C. Wölk*[c], *V. Ziegler*[c], *C. Gässler*[c]<br>(a) University of Applied Sciences Dresden, Friedrich-List-Platz 1, D-01069 Dresden, Germany,<br>(b) Dresden University of Technology, Mommsenstr. 13, D-01062 Dresden, Germany<br>(c) DaimlerChrysler AG, Research and Technology, Wilhelm-Runge-Strasse 1, D-89081 Ulm, Germany |
| **5.50 pm** | **Electron Saturation Velocity in $Ga_{0.52}In_{0.48}P$ as a Function of Temperature in Double Heterojunction Bipolar Transistors**<br>*M. Yee, P.A.Houston and J.P.R. David*<br>Department of Electronic and Electrical Engineering, University of Sheffield, Mappin Street, Sheffield S1 3JD, UK |
| **6.05 pm** | **Non-Destructive Depth-Resolved Characterization of InGaP/GaAs Multi-Layer Heteroepitaxial Wafers by Cathodoluminescence**<br>*F. Ishikawa and H. Hasegawa*<br>Research Center for Integrated Quantum Electronics and Graduate School of Electronics, and Information Engineering, Hokkaido University, Sapporo 060, Japan |
| **6.20 pm** | **Microwave Source Studies based on Reflection Type Oscillators and different HEMT - Circuit Configurations**<br>*A. Megej and H. L. Hartnagel*<br>Technische Universität Darmstadt, Institut für Hochfrequenztechnik, Merckstr. 25, Darmstadt, 64283, Germany |

# Design and Fabrication of Gate and Gate Recess for Ultrahigh-Speed InP-Based HEMTs

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InP-based InAlAs/InGaAs high electron mobility transistors (HEMTs) are the fastest transistors, exhibiting a cutoff frequency ($f_T$) of over 350 GHz [1-3]. Current research interest is divided into two major areas: (i) manufacturability and reliability, focusing on the 40-Gb/s optical-fiber communications and millimeter-wave applications with regard to InP-HEMTs with gate lengths longer than 100 nm, and the further improvement of high-frequency performance for over-100-Gb/s optical communications and (ii) higher frequencies such as the G band (140-220 GHz) regarding sub-100-nm gate devices. Indeed, the highest $f_T$ was achieved by 30-nm-gate HEMTs with a recessed gate structure [3]. As the gate length becomes shorter, the extrinsic gate region (i.e., the gate recess) comes to play an important role in the $f_T$, $f_{max}$, breakdown, and reliability of HEMTs [3,4].

The heterostructure design and gate structure is depicted in Fig. 1. The gate length is defined by the opening at the $SiO_2$ film, which is patterned with e-beam lithography. A fullerene-incorporated nanocomposite e-beam resist [5] was used to achieve extremely short gate length of 30 nm [1]. The gate Schottky contact was deposited on the i-InAlAs by two-step recess etching, i.e., first removing the n-InGaAs/n-InAlAs cap layer by wet etching and then removing the InP layer by dry etching [1]. The InP layer is employed as an etch stop layer for the controllability of the threshold voltage of HEMTs. In addition, the InP recess surface was found to have a passivation effect that suppresses the kink effect and the frequency dispersion of the transconductance [6,7]. The kink effect is modeled by the change in the source resistance (and thus the extrinsic transconductance) caused by the accumulation of holes generated by impact ionization [8]. An electroluminescence study indicated that the generated holes accumulate in the source side of the HEMT [9]. The influence of the hole accumulation was found in the results of a 2D numerical analysis (Fig. 2), in which the I-V characteristics of the 100-nm-gate HEMT models having different hole lifetime are compared. The longer lifetime, which means more accumulation of holes, gives the kink effect and an explosive increase in the drain current (on-state breakdown) at lower drain voltage. With respect to the kink effect, the role of the recess surface is significant. The gate recess covered with InP (Fig. 1) gives the normal I-V characteristics; even the lateral depth of the gate recess ($L_{side}$) exceeds 260 nm (Fig. 3a). When InAlAs is exposed in the gate recess, on the other hand, the collapse of the drain current and the kink effect are observed at $L_{side}$ of 120 nm (Fig. 3b). Due to the carrier depletion caused by the surface pinning, devices with a strong kink effect have a resistive gate recess. The carrier depletion also makes the device characteristics sensitive to the hole accumulation. A light irradiation study, in which the electron-hole pairs are produced by illumination instead of impact ionization, indicated that the decrease in the parasitic resistance primarily increases the drain current and, at large light powers, the drain current is boosted more due to the shift in the threshold voltage that is caused by the positive charges of holes accumulated under the gate (Fig. 4) [10].

The typical high-frequency characteristics of 30-nm-gate HEMTs with $L_{side}$ of 260 nm are shown in Fig. 5. The 20-dB/decade roll-off line gives $f_T$ of 368 GHz, which is the highest $f_T$ ever achieved by any kind of transistor. The gate length dependence of $f_T$ is characterized by $f_T = [2\pi(\tau_{ex} + L_g/v_s)]^{-1}$, where $\tau_{ex}$, $L_g$ and $v_s$ are the extrinsic delay time, gate length and carrier velocity, respectively. The $L_g$-$f_T$ dependence of InP-HEMTs gives $v_s$ of $2.7 \times 10^7$ cm/s, which is larger than that of the other two materials (GaAs and Si in Fig. 6). As $L_g$ becomes shorter, however, the influence of $\tau_{ex}$ becomes more significant as shown in the fitting curves with different $\tau_{ex}$ in Fig. 6. The $\tau_{ex}$ is the delay independent of $L_g$, and consists of the charging time and the transit time to run in the excess gate region ascribed to the difference between the effective and nominal gate length. Evidence of parasitic effects on high-frequency characteristics was observed in the $L_{side}$ dependence of $f_T$, the parasitic resistance ($R_s$) and capacitance ($C_{gd}$) of 30-nm-gate HEMTs (Fig. 7). This result suggests that the maximum $f_T$ is given by $L_{side}$ optimized so as to minimize the contribution of $R_s$ and $C_{gd}$. Since the intrinsic delay $L_g/v_s$ is estimated to be 0.11 ps at $L_g$ = 30 nm, $\tau_{ex}$ becomes the principal factor limiting $f_T$ in such a short gate range. The design of the gate and gate recess structure, therefore, should be improved to suppress these parasitic components, both resistance and capacitance.

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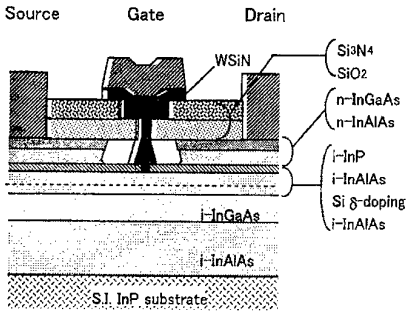



Fig. 1: Schematic cross section of InP-based HEMT.

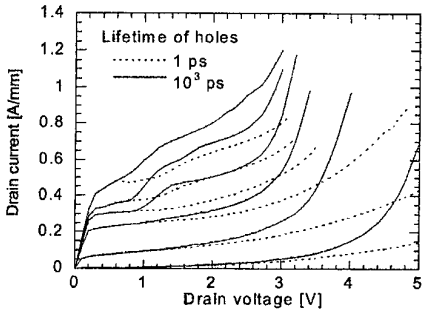
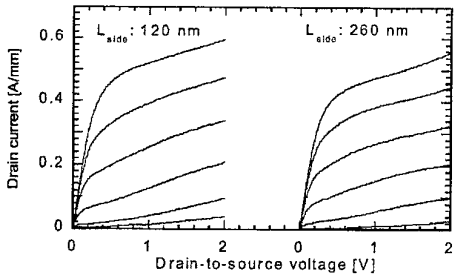
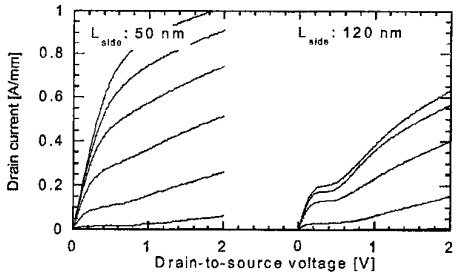



Fig. 2: Numerical analysis of I-V characteristics of 100-nm-gate HEMT with different lifetimes of holes in InGaAs channel (1 and $10^3$ ps). Gate voltages: 0.2 V top, -0.2 V step.




a) Recess surface: InP




b) Recess surface: InAlAs

Fig. 3: Impact of recess surface material of 100-nm-gate InP-HEMTs: a) Recess surface is InP. Gate voltage: 0.4 V top, -0.1 V step. b) Recess surface is InAlAs. Gate voltage: 0.4 V top, -0.2 V step.

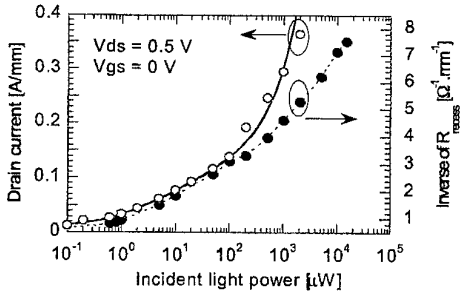



Fig. 4: Light-irradiation-induced change in drain current and gate-recess resistance ($R_{recess}$) of a kink device (InAlAs recess surface with $L_{side}$ = 120 nm) in pre-kink bias (gate voltage and drain voltage are 0 and 0.5 V, respectively).

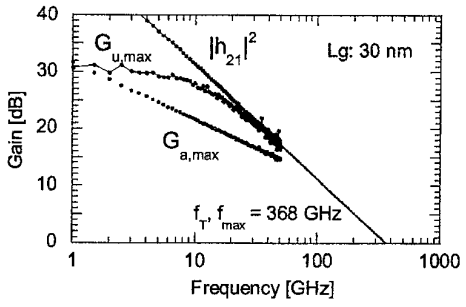



Fig. 5: Typical high-frequency characteristics of 30-nm gate HEMTs. Lateral depth of gate recess ($L_{side}$) is 260 nm. Gate voltage and drain voltage are 0.15 and 0.7 V, respectively.

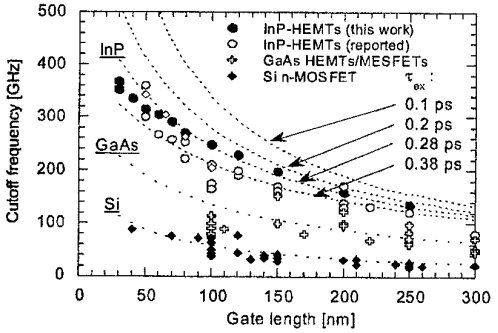



Fig. 6: Gate length dependence of cutoff frequency of FET's based on InP, GaAs and Si. Dotted curves for InP-HEMT are calculated with various extrinsic delay time ($\tau_{ex}$).

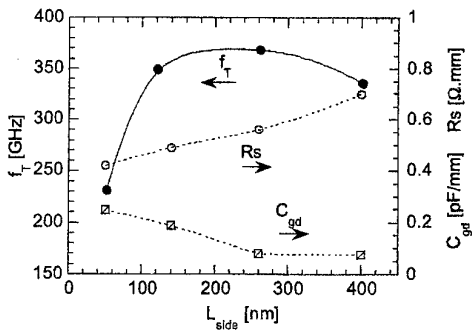



Fig. 7: Cutoff frequency ($f_T$), source resistance ($R_s$) and feedback capacitance ($C_{gd}$) versus lateral depth of gate recess ($L_{side}$) for 30-nm-gate HEMTs.

# Fast Traps in InAlAs/InGaAs/InAlAs/InP 2-DEG Channels

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Channels containing a two-dimensional electron gas (2-DEG) are widely used in high-electron-mobility transistors (HEMTs). An undoped InGaAs quantum-well layer confined between two InAlAs barrier layers supports excellent high-speed low-noise performance of the transistors at millimeter-wave frequency [1]. A drawback of Al-containing structures comes from traps acting at frequencies up to several hundreds of megahertz [2, 3]. No data on the trap origin and location is available; the traps are likely distributed either at the interfaces [2, 4] or in the bulk of InAlAs barrier layer [2, 5]. Our results on microwave noise show that the trap levels in question are located on the substrate side from the InGaAs well. The trap energy is estimated to be near 0.25 eV below the conduction band edge of InAlAs.

The mobile electrons for the investigated InGaAs quantum-well channels are supplied by the donor planes located in the InAlAs barrier layers. Channels 13Q and 14Q have the donor plane on the surface side from the well, channel 15Q has two donor planes on the both sides. The typical 2-DEG densities and electron mobilities at 77 K are 2.4 $10^{12}$ $cm^{-2}$ and 37 000 $cm^2/(V\ s)$ for the one-side-doped channels (13Q and 14Q) and 4.3 $10^{12}$ $cm^{-2}$ and 11 900 $cm^2/(V\ s)$ in the case of two-side doping (channel 15Q). Channel 13Q contains lattice-matched InGaAs (53% of InAs), channel 15Q contains strained InGaAs (70% of InAs), and channel 14Q combines layers with 53% and 70% of InAs.

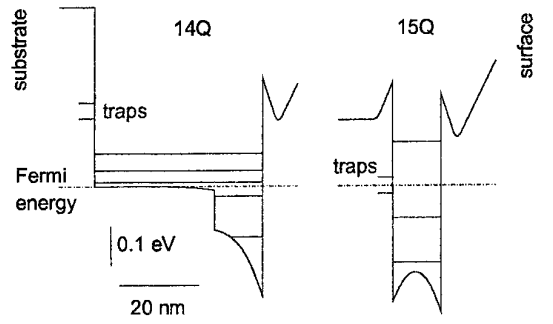


*Fig. 1. Subband diagrams for one-side-doped (14Q) and two-side-doped (15Q) channels.*

The subband energies and the Fermi energy are studied using a self-consistent solution of the coupled Schrödinger-Poisson equations, taking into account the subband occupation at 80 K (Fig. 1). According to the calculations, the mobile electrons occupy the lowest two subbands.

Noise temperature is measured in 0.22–10 GHz frequency range at 80 K temperature using coaxial and waveguide radiometric techniques (for details see, for example, [1]).

The generation–recombination noise is observed at microwave and lower frequencies (Fig. 2). In the two-side-doped heterostructure 15Q, this noise dominates in the wide range of electric fields (Fig. 3) indicating that the thermal equilibrium electrons interact with traps as well as the hot electrons do. The noise source with similar cutoff frequencies is essentially weaker in the one-side-doped channels at low and moderate electric fields (Fig. 3), but the source is strong at high electric fields (Fig. 2, 14Q). The lattice strain is not a prerequisite for formation of the trap levels in question: channel 14Q shows the noise behaviour similar to that of the lattice-matched one 13Q (Fig. 3). Consequently, for channels 13Q and 14Q, the electrons must be hot to be trapped.

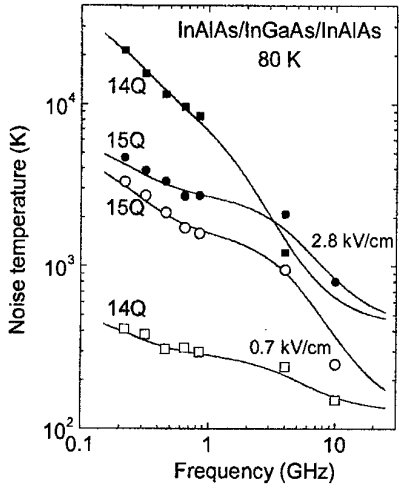


*Fig. 2. Frequency-dependent noise temperature for channels 14Q (squares) and 15Q (circles) at different electric field: moderate (open symbols) and high (closed symbols).*

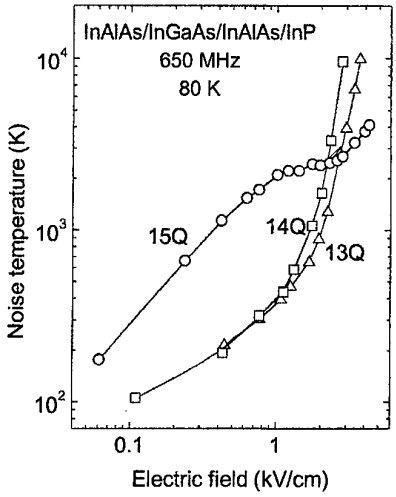


*Fig. 3. Field-dependent noise temperature at 650 MHz for different channels: lattice-matched (13Q, triangles), splitted (14Q, squares), and strained (15Q, circles).*

The experimental data show that, for the two-side-doped channel 15Q, the electrons can be trapped already at thermal equilibrium and at low electric fields. This is possible if the trap level energy is almost equal the Fermi energy. Since the electrons are confined in the quantum well, the traps might be located either on the heterointerfaces or in the bulk of InAlAs near the heterointerfaces. In the latter case electron tunneling takes part. Figure 2 shows that the experimental data can be fitted by the sum of two Lorentz-type contributions with essentially different cutoff frequencies (200 MHz and 1.5–4 GHz) superimposed onto the almost 'white' contribution due to the hot-electron velocity fluctuations. This result is in line with essentially different confinement of the electrons occupying the lowest two subbands. It is believed that the less-confined electrons undergo a faster trapping assisted by tunneling. Assuming that the conduction band offset equals 0.55eV, data of Fig. 1 (15Q) suggest that the trap levels are at about 0.25 eV below the conduction band of InAlAs.

An additional information is available from the noise data obtained for the one-side-doped channels 13Q and 14Q. In absence of the donor plane on the substrate side, the conduction band of the InAlAs layer moves upward in respect to the Fermi level (Fig. 1). The traps, located on or near this interface, move up as well. They become out of reach for the equilibrium electrons. Since we observe that the generation–recombination noise is quite weak at low electric fields in channels 13Q and 14Q (Fig. 3), the traps on the surface side should be excluded from the consideration. The remaining traps are those located on the substrate side high above the Fermi level. This conclusion is supported by the experimental data on the generation–recombination noise arising at high electric fields in one-side-doped channels: only high-energy electrons can be trapped efficiently (see 14Q in Fig. 2).

Support under Contract V-019-2001 of the Lithuanian National Science and Education Foundation is acknowledged.

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# Evaluation of $SiN_x$ Passivation on InP HEMTs at Room and Cryogenic Temperature

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**Abstract — The performances of surface passivated and non-passivated InP high electron mobility transistors (HEMTs) are presented. After adding a $SiN_x$ passivation layer a shift of the threshold voltage $V_{th}$ from -0.35V to -0.25V and an increase in the maximum transconductance $G_{M,max}$ of 5% was observed. A similar behavior can be seen with non-passivated devices after a certain storage time. A comparison of the rf and noise performances shows no significant degradation after passivation.**

## 1. Introduction

In certain applications like radio astronomy and deep space communication there is a need for receivers with high sensitivity and ultimate noise performance. Most receivers in these applications make use of cryogenic amplifiers with GaAs or InP HEMT devices in the front-end. InP HEMT devices are preferred devices for millimeter-wave frequency applications, whereas they are not very often used in receivers at lower microwave frequencies. Work has been carried out to improve gain and noise performances of InP HEMTs at room and cryogenic temperatures. The work presented in [1] shows a possible advantage of InP HEMTs over GaAs HEMTs at lower microwave frequencies with regard to cryogenic noise performance.

To avoid a degradation of the device performances and to stabilize the T-gate mechanically, a $SiN_x$ passivation layer has been applied. In this paper, we present a comparison of passivated and non-passivated devices in regard to dc, rf and noise performances. All measurements are based on devices with bondable pads.

## 2. Device Fabrication

The HEMT structure studied in this work consists of an n-doped $In_{0.53}Ga_{0.47}As$ cap layer, an $In_{0.52}Al_{0.48}As$ Schottky barrier layer, a Si-δ doping plane, an $In_{0.52}Al_{0.48}As$ spacer, an $In_{0.53}Ga_{0.47}As$ channel and an $In_{0.52}Al_{0.48}As$ buffer layer.

The devices have a gate length of 0.2μm and a gate width of 2x75μm. The T-shaped gate was defined by an electron beam lithography process with a triple PMMA-based resist layer stack. Gate recess through the $In_{0.53}Ga_{0.47}As$ cap layer was done using a highly selective wet chemical etching process. A cross-section of the device is shown in Figure 1.

The $SiN_x$ coating of the passivated devices has a thickness of 130 nm. The nitride was deposited by plasma enhanced chemical vapor deposition (PECVD) at 120°C with a deposition rate of 14 nm/min. The passivation layer was applied over the gate and part of the ohmic contacts. To study the effect of this passivation, two chips have been produced in the same run. The $SiN_x$ passivation layer has been applied to one of the chips.

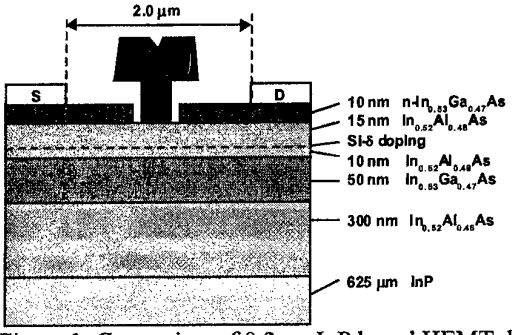


Figure 1: Cross-view of 0.2μm InP based HEMT device

## 3. Measurement Results

Prior to the $SiN_x$ passivation DC measurements were carried out. After the passivation DC characteristics show a shift of the threshold voltage $V_{th}$ from -0.35V to –0.25V and an increase in the maximum transconductance $G_{M,max}$ of 5% (see Figure 2). This effect is likely due to a change of the surface potential caused by the $SiN_x$ passivation layer.

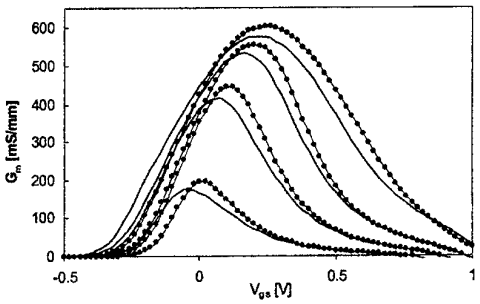


Figure 2: Transconductance $G_m$ [mS/mm] before (line) and after (dots) $SiN_x$ passivation

While DC parameters do not vary with time on devices after passivation, they do on non-passivated ones. An increase of $G_{M,max}$ and a shift of $V_{th}$ can be observed on non-passivated devices. Figure 3 shows this behavior after a period of four months. A possible explanation is that the natural oxidation of the surface of the InAlAs Schottky layer of the non-passivated HEMTs finally originates a similar change in DC characteristics of the devices as device passivation. After four months, a further comparison of rf s-parameters and cut-off frequency $f_T$ (see Figure 4) confirms the similar behavior of the passivated and non-passivated devices.

No significant differences between the two types can be noted.

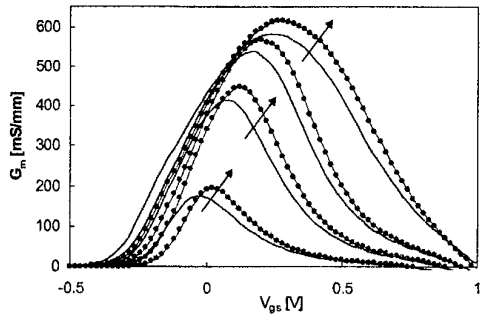


Figure 3: Shift in transconductance $G_m$ [mS/mm] of non-passivated HEMTs over a period of four months

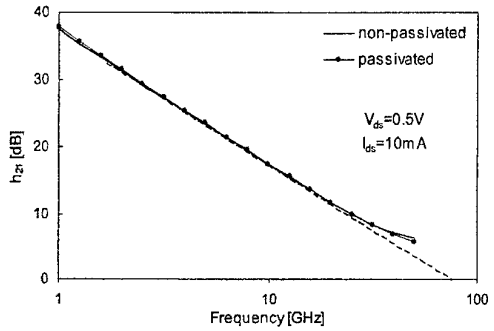


Figure 4: Measured $h_{21}$ at room temperature of a passivated (dots) and non-passivated (line) device at $V_{ds}$=0.5V and $I_{ds}$=10mA (with pad parasitics included)

The noise performances at room and cryogenic temperatures were our main criterion of studying the influence of device passivation. The measured minimum noise figure $F_{min}$ at room temperature is shown in Figure 5. In the lower GHz range a slight improvement of the noise performance of passivated devices can be noted. It is presumed that the passivation reduces the surface trapping effects which has a positive impact on the noise performance. The noise measurements were done at the same bias conditions of $V_{ds}$=0.5V and $I_{ds}$=10mA.

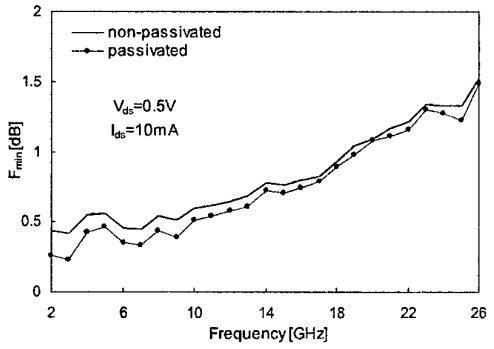


Figure 5: Minimum noise figure $F_{min}$ at room temperature of passivated and non-passivated devices at $V_{ds}$=0.5V and $I_{ds}$=10mA

Our noise parameter measurement system allows $F_{min}$ measurements at room temperature only. At cryogenic temperature, the noise temperatures $T_n$ of hybrid two-stage amplifiers have been measured, fabricated with passivated and non-passivated devices. Initially the first and second stages of the amplifier were fabricated with non-passivated devices. Then, the non-passivated device of the first stage was replaced by a passivated one. The noise performances were measured with both configurations. Figure 6 shows the noise temperature $T_n$ of a two-stage hybrid amplifier. No significant shift in $T_n$ can be seen.

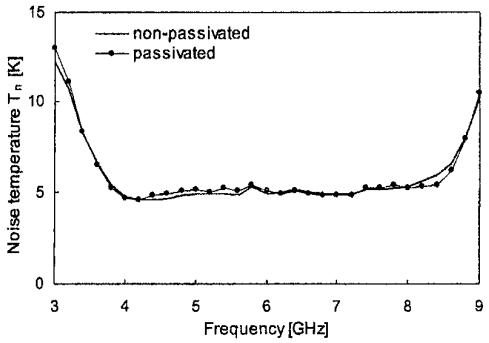


Figure 6: Noise temperature $T_n$ of two-stage amplifiers with passivated (dots) and non-passivated (line) devices at cryogenic temperature (15 K)

## 4. Conclusions

A comparison of the device performances of passivated and non-passivated InP HEMT devices shows an improvement of the passivated devices in terms of time stability. While DC characteristics do not vary with time for passivated devices, they do for non-passivated ones. Additionally, rf and noise performances show no significant differences between the two devices. A slight improvement of the noise performance at lower microwave frequencies for the passivated devices can also be noted. In order to further investigate the effect of passivation and aging low frequency noise measurements will be performed.

## 5. Acknowledgment

The authors would like to thank H.P. Meier and Bruno Graf for processing the devices and J.D. Gallego with Centro Astronomico de Yebes, Spain for performing the cryogenic noise measurements.

## 6. References

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# Simulation of Ultra Short Channel InAlAs/InGaAs/InP High Electron Mobility Transistors by a Coupled Solution of the Schrödinger Equation with a Hydrodynamic Transport Model

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The simulation and measurement of ultra short channel high electron mobility transistors (HEMT), based on InAlAs/InGaAs/InP, are presented. These structures are experimentally investigated at the DaimlerChrysler AG. For the simulation the device simulator SIMBA is used, where several physical models (e.g. drift diffusion (DD) model, hydrodynamic (HD) transport model and a coupled solution of the Schrödinger equation [1] with a HD transport model) are included.
The device structure used for the simulation is represented in Fig. 1 together with the doping densities. Fig. 2 and Fig. 3 show the calculated output and transfer characteristics, respectively. Additionally the results of a HD transport model and measurement data are inserted. Essential physical effects (e.g. short-channel and overshoot effects), which determine the behavior of the HEMT structure, can be identified in the corresponding device characteristics. The difference between the simulation models consists in the computation of the electron density at the hetero interface, which was exactly calculated by a solution of the Schrödinger equation with a HD transport model. Fig. 4 shows the power gain as a function of frequency (MSG/MAG). The transit frequency $f_T$ = 132 GHz and the maximum frequency of oscillation $f_{max}$ = 176 GHz are obtained by a dynamic simulation at the working point $V_{DS}$ = 1.1 V and $V_{GS}$ = -0.3 V. In this point the device possesses the maximum transconductance with $g_m$ = 760 mS/mm.
The capability of device simulation contains the possibility to investigate scaling effects. The performance, especially the output and transfer characteristic, of InAlAs-based HEMT has been evaluated as a function of gate length ($l_G$) in the range from $l_G$ = 7 nm to $l_G$ = 120 nm and for a corresponding scale of vertical dimensions. In Fig. 5 the output characteristic are illustrated for different gate lengths at $V_{GS}$ = 0.

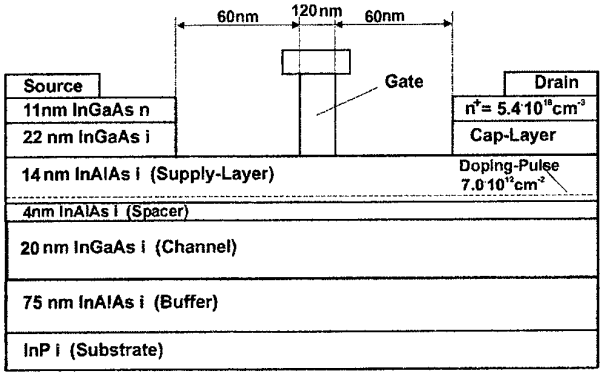


**Fig. 1 Structure of the InAlAs/InGaAs/InP-HEMT**

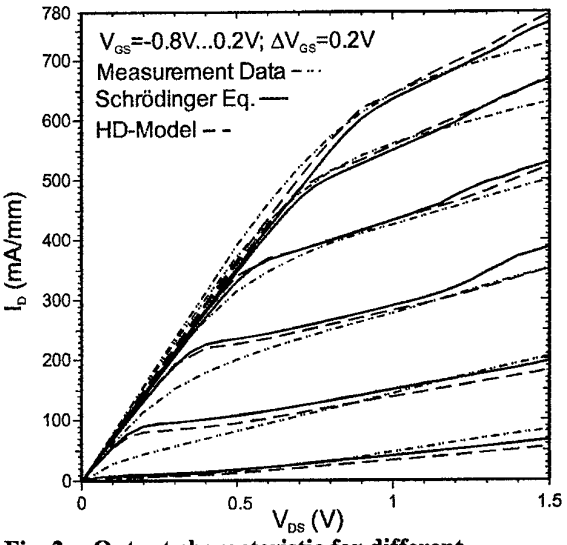


**Fig. 2 Output characteristic for different simulations models**

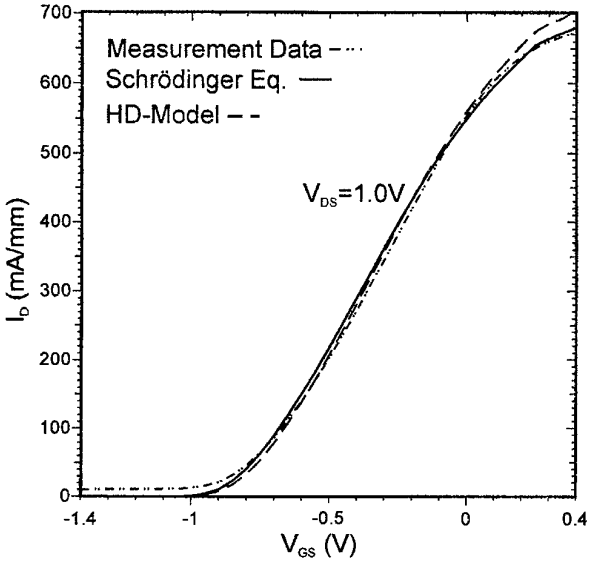


**Fig. 3 Transfer characteristic for different simulations models**

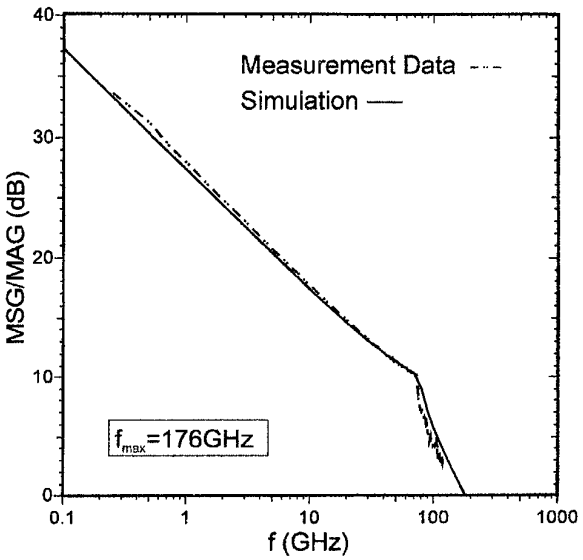


**Fig. 4 Calculated and experimental results of MSG/MAG ($V_{DS}$ = 1.1 V; $V_{GS}$ = -0.3 V)**

The behavior at extremely short gate lengths shows essential scaling effects like short-channel and overshoot behavior. As a result of dynamic simulation at the working point $V_{DS}$ = 1.1 V, $V_{GS}$ = -0.3 V for a 60 nm gate length $f_{max}$ = 650 GHz was obtained. With the 30 nm gate length device $f_{max}$ = 710 GHz can be achieved. The gate to channel aspect ratio, the threshold voltage and the maximum transconductance, for the gate lengths in the range from $l_G$ = 7 nm to $l_G$ = 120 nm, are summarized in Table 1.

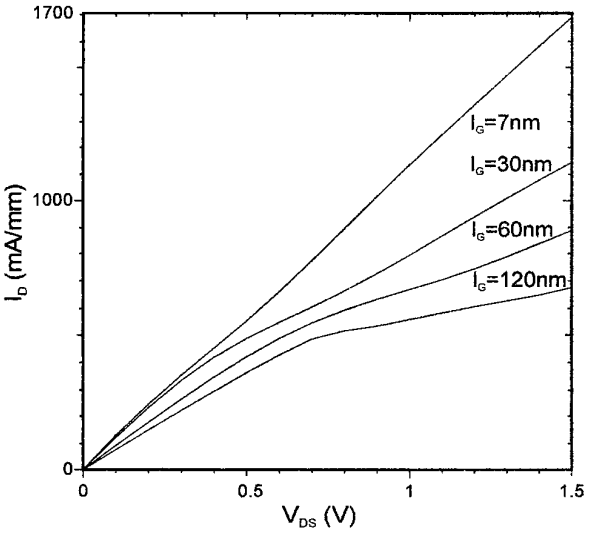


**Fig. 5 Output characteristic for different gate lengths at $V_{GS}$ = 0**

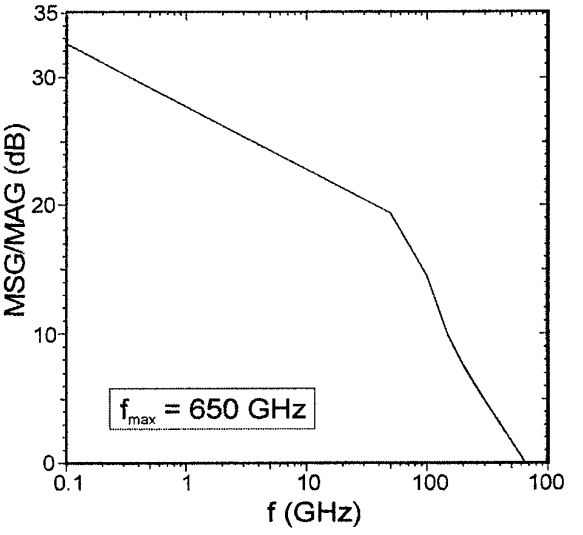


**Fig. 6 MSG/MAG for the HEMT-Structure with $l_G$ = 60 nm ($V_{DS}$ = 1.1 V; $V_{GS}$ = -0.3 V)**

**Table 1 Parameters of the ultra short channel InAlAs/InGaAs/InP-HEMTs**

| Gate length $l_G$ (nm) | 7 | 15 | 30 | 60 | 120 |
|---|---|---|---|---|---|
| Gate to channel aspect ratio | 2.33 | 3.0 | 3.0 | 4.0 | 6.66 |
| Threshold voltage $V_{th}$ (V) | -0.85 | -0.75 | -0.9 | -1.1 | -0.9 |
| Maximum transconductance $g_m$ (mS/mm) | 2600 | 2225 | 1875 | 750 | 738 |

[1] C. Pigorsch, W. Klix, R. Stenzel. Microelectronic Engineering, **43-44** (1998), pp. 325-333

# Electron Saturation Velocity in $Ga_{0.52}In_{0.48}P$ as a Function of Temperature in Double Heterojunction Bipolar Transistors

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## Introduction

Heterojunction Bipolar Transistors (HBTs) are recognised as useful devices for high power and high speed operation. Crucial to defining the frequency limits of operation is a knowledge of electron saturation velocity in the collector over the range of operating temperatures. As the collector current in the HBT increases, the electric field at the base edge of the junction aproaches zero. When the electric field at that junction reaches zero, holes from the heavily doped base spill over into the collector, compensating the negative charges, thus prevent the electric field from becoming positive. Any further increase in the collector current results in the formation of a 'base push-out' region [1]. This increase in minority-carrier charge storage in the base causes a degradation in current gain ß of the device and hence limits the current density in the device. The onset of 'base push-out' occurs at the Kirk current density, $J_K$, given by,

$$J_K = qv_{sat}\left[Nc + \frac{2\epsilon(V_{CB}+V_{bi}-R_CI_C+R_BI_B)}{qW_C^2}\right] \quad (1)$$

where $q$ is the electron charge, $v_{sat}$ is the saturation velocity, $V_{CB}$ is the applied collector-base voltage, $V_{bi}$ the collector-base built-in voltage, $\epsilon$ is the permittivity of the collector, $R_C$ and $R_B$ the collector and base series resistance respectively, $N_C$ is the collector doping density and $W_C$ the collector layer thickness of doping $N_C$. $(V_{CB}+V_{bi}-R_CI_C+R_BI_B)$ is the base-collector junction voltage, which allows for the voltage drop across the resistance between the contacts and the junction as shown in Figure 1.

In this work, we report the first direct measurement of electron saturation velocity in GaInP using the Kirk Effect as a function of temperature.

## Experiment

A graded base $Ga_{0.52}In_{0.48}P$/AlGaAs-/$Ga_{0.52}In_{0.48}P$ Double Heterojunction Bipolar Transistor (DHBT) with aluminium mole fraction varying from 0.11 at the collector end to 0.21 at the emitter end is used to determine the electron saturation velocity of GaInP. The 0.11 Al composition at the collector end ensured a zero conduction band spike there [2]. Pulse biasing the DHBT (typical pulse length of 1ms with pulse repetition frequency of 1 s) was done to minimise device self-heating. The current density for the onset of base push-out, i.e. Kirk current density, can be determined when the current gain falls with increasing collector current (Figure 2).

Figure 3 shows measured Kirk current density as a function of applied collector-base voltage of a $Ga_{0.52}In_{0.48}P$/AlGaAs/$Ga_{0.52}In_{0.48}P$ DHBT at temperatures of 22°C to 200°C. The resultant electron velocity saturation of GaInP against temperature is obtained from the slopes of Figure 3 and is shown in Figure 4.

The advantage of measuring the Kirk current, as a function of $V_{CB}$ is that the saturation velocity can be determined from the gradient of the $J_K$ versus $V_{CB}$ characteristics. This procedure is independent of the collector doping density and hence eliminates the need to measure it accurately.

An electron saturation velocity of 4.6 x $10^6$ cm/s was obtained at room temperature. Figure 4 also shows that the electron saturation velocity decreases rapidly with increasing temperature. This rapid decrease has important implications for the

deterioration of frequency performance of HBTs in this materials system at normal operating temperatures in power applications.


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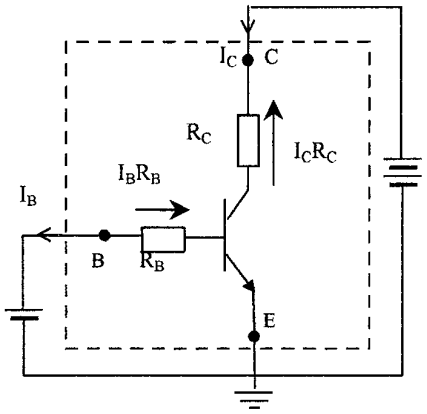


Figure 1: HBT in common-emitter configuration with internal base and collector series resistance.

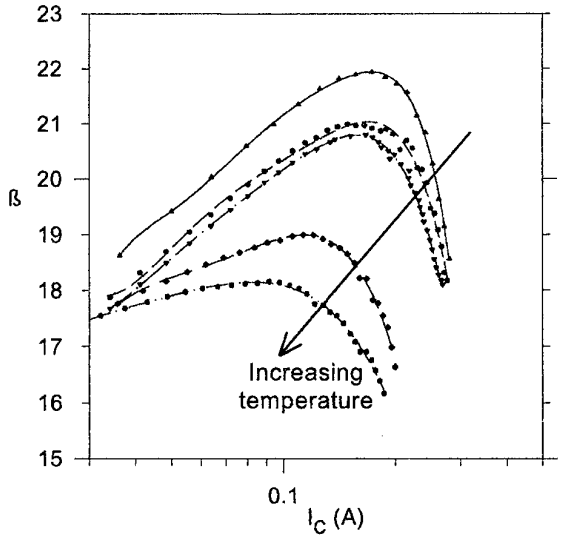


Figure 2: Current gain versus collector current at 20°C, 60°C, 100°C, 150°C and

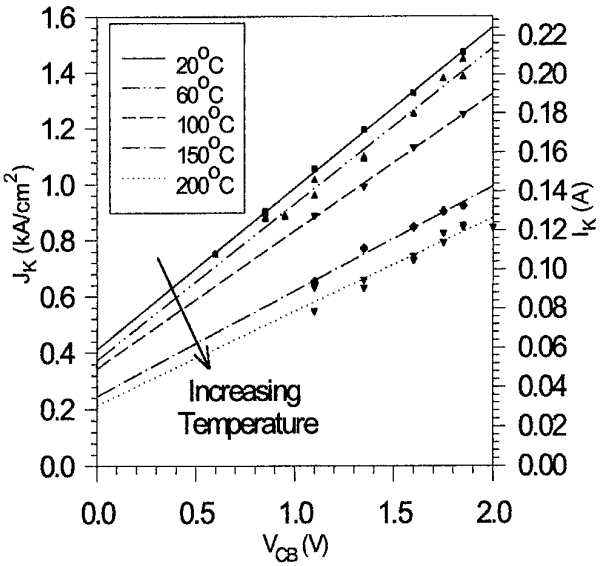


Figure 3: Temperature dependent Kirk current density ($J_K$) and Kirk current ($I_K$) at various collector-base biases.

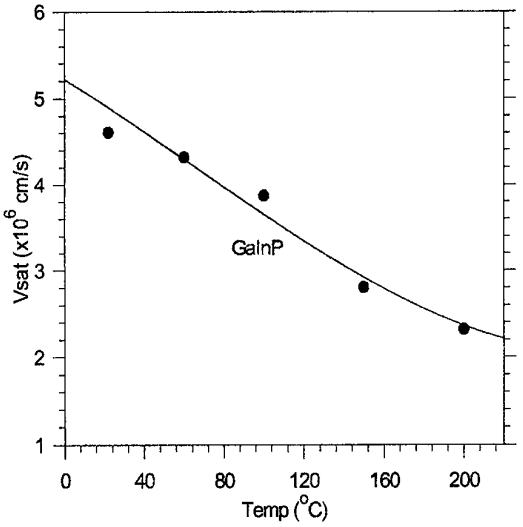


Figure 4: Variation of electron saturation velocity with temperature in $Ga_{0.52}In_{0.48}P$

# Non-Destructive Depth-Resolved Characterization of InGaP/GaAs Multi-Layer Heteroepitaxial Wafers by Cathodeluminescence

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Depth-resolved cathodeluminescence is shown to be a powerful technique for contactless, non-destructive characterization of advanced multi-layer heteroepitaxial wafers.

## Introduction

For research as well as mass production of advanced heterostructure devices, a method for non-destructive, highly sensitive and non time-consuming characterization of buried hetero-structure layers and their interfaces in epitaxial wafers is strongly desired. Cathodeluminescence□(CL) allows depth-resolved measurements by changing acceleration voltage, leading to characterization of carrier profiles, surface and bulk deep states, Schottky interfaces, often by name of LEEN[1]. However, application to heterointerfaces has not been made.

The purpose of this paper is to demonstrate a cathodeluminescence interface spectroscopy (CLIS) technique as a powerful contactless and non-destructive characterization method of multi-layer heteroepitaxial structures through the results taken on various InGaP/GaAs multilayer heteroepitaxial wafers.

## Principle and Theoretical Analysis

The principle of the CLIS technique for a simple heterostructure consisting of two materials A and B is schematically shown in **Fig.1**. The structure gives, at an electron acceleration voltage, $V_{acc}$, two near-bandgap CL peaks with peak intensities $I_A(V_{acc})$ and $I_B(V_{acc})$. Since the penetration depth of electons is strongly dependent on $V_{acc}$, $I_A$ and $I_B$ depend also strongly on $V_{acc}$. Plots of $I_A(V_{acc})$ and $I_B(V_{acc})$ vs. $V_{acc}$ are defined as CLIS spectra. If CLIS spectra for the ideal case without any defects are known by a detailed computer simulation, or by experiments on near-ideal reference samples, then any deviations in measured spectra from ideal CLIS spectra such as change in spectra shapes and intensities, and/or appearance of unexpected CL peaks, indicate that some unwanted anomalies are present in the heterostructure. Then, by a subsequent computer analysis, it should be possible to identify the causes of the anomalies.

For theoretical analysis of CLIS spectra, a 1D Scharfetter-Gummel vector-matrix type self-consistent semiconductor simulation program which our group developed for analysis of photoluminescence[2] was modified to obtain CLIS spectra. Excitation by incident electrons was obtained by calculating the Everhart-Hoff electron energy loss curve[3].

## Feasibility Study

In order to experimentally investigate the feasibility of the CLIS technique, a well characterized commercial high quality InGaP/GaAs single heterostruacture grown by MOVPE was investigated. Two peaks A and B coming from InGaP and GaAs were seen, as shown in **Fig.2(a)**, and the CLIS spectra shown in **Fig.2(b)** agreed well with the theoretical analysis.

## Application to Multi-Layer Wafers

InGaP/GaAs single heterostructure and quantum well samples were grown by gas source molecular beam epitaxy (GSMBE) using tertiarybutylphosphine as the P source[4]. These samples showed existence of anomalous peaks in addition to the expected GaAs peak, the InGaP peak and the QW peak. From the theoretical analysis of their CLIS spectra, the anomalous peaks were found to come from the InGaP/GaAs interfaces, suggesting formation of P-vacancy related interface defects due to improper group V switching. In fact, under the optimal growth condition, these peaks could be removed. Finally, the CLIS technique was applied to MOVPE grown HBT wafers. Observed CL and CLIS spectra are shown in **Fig.3(a)** and **(b)**. Four CL peaks were observed. From their CLIS spectra as well as their energy positions, they were assigned to the InGaP/GaAs interface related "deep emission" peak, the GaAs-base band edge emission peak, the GaAs-base C-related exciton emission peak and the GaAs $n^+$ sub-collector peak, respectively.


[1] T.M.Levin, G.H.Jessen, F.A.Ponce and L.J.Brillson, J.Vac.Sci.&Technol. B **17** (1999) 2545.
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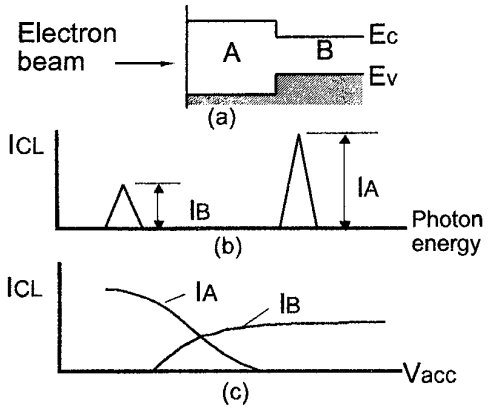


**Fig.1** Principle of CLIS technique.

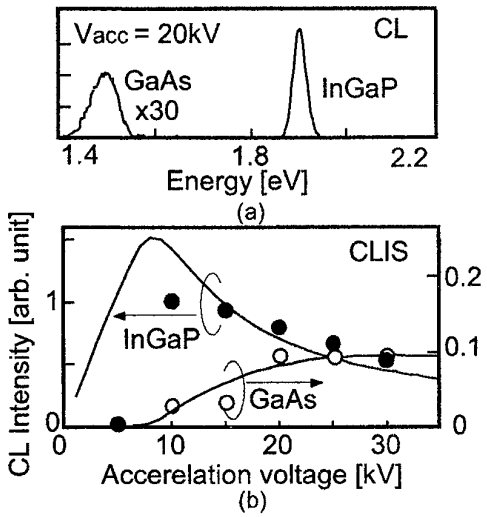


**Fig.2** (a) CL and (b) CLIS spectra from a reference sample.

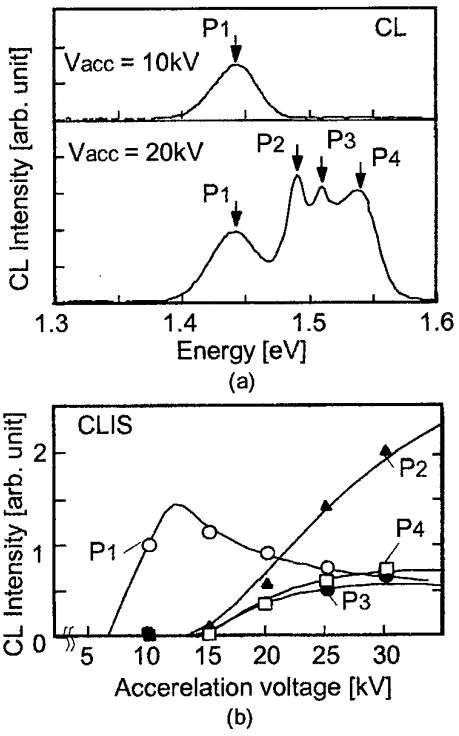


**Fig.3** (a) CL and (b) CLIS spectra from an MOVPE HBT wafer.

# Microwave Source Studies Based on Reflection-Type Oscillators and Different HEMT-Circuit Configurations

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## Abstract

**A systematic study of maximally broadband VCO designs is undertaken. The theoretical efforts lead to the practical realization of two fully monolithically integrated VCOs based on the reflection-type technique. Employing the diode tuning, the practical realizations of PHEMT-MMICs exhibit 14% and 28% bandwidth of oscillations.**

## Introduction

Wide-band voltage-controlled oscillators are an essential part in a variety of applications. The increasing use of the monolithically integrated circuits (MMIC's) has created the need for high-performance MMIC-VCO's. Further, HEMT oscillators are needed if they have to be integrated with HEMT amplifiers, mixers, and detectors to form a single-chip system.

The objective of this paper is to analyse two different approaches to the reflection-type VCO designs, namely the common-drain and common-source techniques and to describe two practical fully monolithically integrated implementations. The negative resistance approach was chosen due to its relative design and analysis simplicity. The measured relative bandwidth of operation covered by single circuits varies within the range of more than 13% up to almost 28%, which are excellent results for these kind of devices.

The circuits were manufactured using the commercially available 0.25 µm pHEMT process PH25 of UMS[1].

## Circuit Designs Considered

*Common-Drain Oscillator*

Oscillators based on the transistors in the so-called "reverse-channel configurations" were first proposed by Wade [1]. The drain terminal of a transistor in that case is biased with a negative voltage, thereby making it to the electrical source. In this way, the disadvantages of other basic configurations–especially in connection with the heat sinking–can be overcome. Further, the magnitude of the transistor input coefficient becomes greater than unity **below** a certain frequency.

In this work, the VCO implementation is presented that is based on a real common-gate transistor configuration. As the feedback element, which helps to achieve the negative differential resistance at the input, acts the gate-source capacitance of the active pHEMT. The simulation results demonstrated that the transistor is already unstable without any additional elements. Furthermore, the magnitude of the input reflection coefficient is greater than unity **above** a certain frequency. Due to this effect, the unwanted low-frequency oscillations can easily be suppressed. Although the forward gain of a common-source configuration is very low, it falls off very gradually with frequency. Therefore, constant performance over a wide range is possible.

The basic schematic of this oscillator is shown in Fig. 1 including the biasing network. An 8×75 µm pHEMT acts as the active device within this circuit. Another small 1×75 µm provides the DC to RF separation over a wide frequency range. The capacitor $C_{FB}$ suppresses the circuit instability at higher frequency values. Inductors $L_{RF}$ and capacitors $C_{RF}$ realize further necessary bias networks.

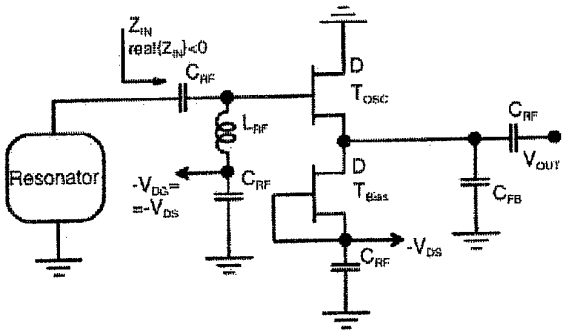


Fig. 1. Basic schematic of the VCO with the oscillating pHEMT in common-drain configuration *(TUD DES 1.1)*.

*Oscillator with Capacitively Induced Negative Resistance*

This kind of oscillators has often been used for microwave circuit design [2]. The disadvantage of this concept is the very difficult bias supply. For this circuit, one needs two bias networks: in the source and in the drain paths of the transistor. Thus, the problem in connection with the DC supply doubles. In our case, we use again the active biasing approach. A very small 1×30 µm pHEMT acts as a current source for a bigger 6×40 µm oscillating transistor. The operation point of the active device changes significantly, but its high-frequency behaviour is still very well suitable for the

[1] United Monolithic Semiconductors, Ulm/Germany and Orsay Cedex/France

oscillator design. The basic schematic of this oscillator is shown in Fig. 2.
It can be shown mathematically [3] that for maximal bandwidth of oscillations the smallest transistor $T_{OSC}$ and capacitance $C_{FB}$ have to be chosen.

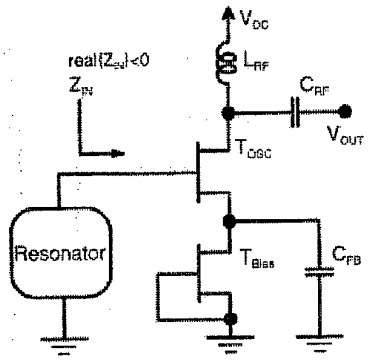


Fig. 2. Basic schematic of the VCO with capacitively induced negative resistance *(TUD DES 1.3)*.

*Measured Results*

On-wafer measurements of the circuits (VCOs including the corresponding buffer amplifiers) were performed employing the spectrum analyser HP8565E. Figures 3 and 4 show measured curves of the oscillation frequency and the output power of buffered VCO realizations in comparison to each other. The summary of the measured performance can be found in Table I.

TABLE I
MEASURED CHARACTERISTICS OF THE VCO'S MANUFACTURED

| | | DES 1.1 | DES1.3 |
|---|---|---|---|
| Frequency Range | $f$ / GHz | 5.21-5.98 | 4.61-6.09 |
| Relative Bandwidth | $\Delta f/f_0$ / % | 13.8 | 27.7 |
| Output Power | $P_{out}$ / dBm | 8.3-10.3 | 11.2-15.5 |

The measured results show that the oscillator based on the common-source transistor with capacitive feedback achieves larger bandwidth of oscillations and higher values of the output power. On the other hand, the power course of the common-drain oscillator is flatter.

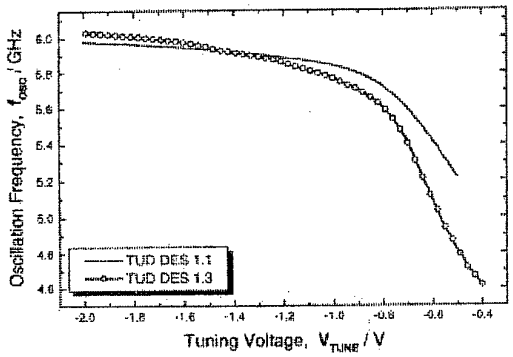


Fig. 3. Measured frequency of the manufactured voltage-controlled oscillators.

Further advantage of the common-drain arrangement is the better heat-sinking since, in this case, one terminal of the transistor is directly connected to the ground.

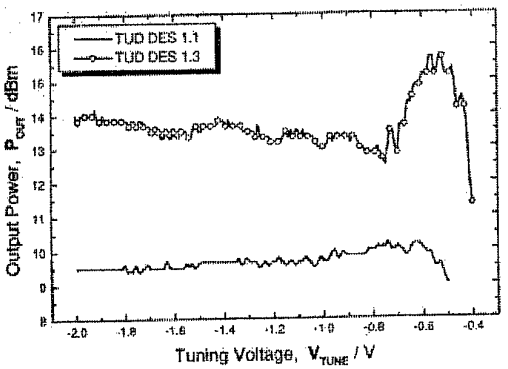


Fig. 4. Measured output power of the circuits investigated

## Conclusions

In this paper, the detailed analysis was applied to the reflection-type VCO design technique with the aim to increase the frequency bandwidth of oscillations. In particular, the commonly used common-source arrangement with capacitively induced negative resistance and the common-drain arrangement were compared to each other.
Further, two practical oscillator realizations are presented and their measured performance is discussed. Incorporating integrated planar PHEMT-diode tuning, the circuits provide frequency tuning in a wide frequency range with almost 14% and 28% relative bandwidth, which are very good results for these kind of circuits.

## Acknowledgement

This work was supported by the ADAM OPEL AG, Rüsselsheim, Germany.

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# SESSION V
# NIGHT POSTER (and Cheese) SESSION
# Monday May 28, 2001

**Theoretical Investigation of Hot Electron Effects in InP-based HEMTs**
*A. Sleiman[(a)], L. Ferranti[(a)], A. Di Carlo[(a)], P. Lugli[(a)] and G. Zandler[(b)]*
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**The significant differences of Al2O3 (0001) substrate nitridation by a nitrogen radio frequency plasma source at high and low substrate temperatures**
*S. Mikroulis[(a)], M. Zervos[(a)], V. Cimalla[(a)], M. Androulidaki[(a)], A. Kostopoulos[(a)], Ph. Komninou[(b)], M. Calamiotou[(c)] and A. Georgakilas[(a)]*
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(c) 3University of Athens, Physics Department, 157 84 Zografos, Greece

**Low temperature-grown Be-doped GaAs for ultrafast optoelectronic applications**
*S. Marcinkevicius[(a)], J. Siegert[(a)], A. Gaarder[(a)], F. Garet[(b)], K. Bertulis[(c)] and A. Krotkus[(c)]*
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(b) LAHC-University of Savoie, 73 376 Le Bourget du Lac Cedex, France
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**Properties of InAs/GaAs lasers grown by MOCVD – application to ridge-waveguide geometry.**
*L.Kuna[(a)], F. Uherek[(a,b)], J.Kováč[(a,b)], A. Vincze[(a,b)], J.Jakabovič[(a)], V.Gottschalch[(c)]*
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(b) Fakultät für Chemie und Physik, Universität Leipzig, Linnéstr.3-5, D-04103 Leipzig, Germany

**Tunable Laser Diodes based on the Quantum Confined Stark Effect**
*N.Le Thomas[(a)], N.T. Pelekanos[(b)], Z.Hatzopoulos[(b)], P. Gilet[(c)], R. Hamelin[(c)]*
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**Current Collapse in AlGaN/GaN HEMTs**
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**Monte Carlo simulation of short channel MOSFETs in 3C, 4H, and 6H-SiC**
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Institut d'Electronique et de Microélectronique du Nord, UMR-C.N.R.S 8520, Département Hyperfréquences et Semiconducteurs (D.H.S) Université des Sciences et Technologie de Lille, Avenue Poincaré, B.P. 69, 59652 Villeneuve d'ascq Cedex, France

**60GHz 420mW/mm Low Gate Current GaInAs/InP Composite Channel HEMT on InP substrate.**
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# Theoretical Investigation of Hot Electron Effects in InP-based HEMTs

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InP-based high electron mobility transistors (InP-HEMTs) have demonstrated excellent high-frequency and high-gain performance [1]. Low breakdown voltage due to hot electron phenomena remains the important disadvantage which limit the power applications of these HEMTs. In this work a proper device design to enhance the breakdown voltage of InP-HEMTs have been theoreticaly investigated.

It has been demonstrated that under near breakdown condition accumulation of holes generated by impact ionization takes place in the gate source channel region, and, in the lower layer and substrate; these clouds of holes gives rise to an enhanced drain current via a parasitic bipolar effect (PBE) [2].

In order to quench the breakdown effect and increase the range of the usable drain voltage in InP-based lattice matched HEMT (InP-LMHEMT) the approach of a body contact (BC) [3] has been adopted. In this communication a 0.25μm double heterojunction InP-LMHEMT with a BC has been investigated by using a Monte Carlo simulator [2,3].

Figure 1 presents the schematic cross section of the InP-LMHEMT with body contact. The BC is formed by an ohmic back contact which extend over the whole bottom of the device and a heavily p-type doped substrate with acceptor density $N_A$.

Figure 2 shows the I/V characteristics of the InP-LMHEMT obtained in off-state $V_{GS}$=-2.0 V and for various situations. The curve labeled without BC shows the current response for the InP-LMHEMT without BC, i.e a LM-HEMT with an undoped InP substrate and without the ohmic back contact. The drain current shows a quick increase and goes directly to breakdown for $V_{DS}$=4V. By considering the InP-LMHEMT with a BC $N_A=5\times10^{18}$ $cm^{-3}$ (dashed line) the breakdown voltage has been shifted towards higher voltage. Thus the BC improves the behaviour of the drain current in near breakdown condition and prevents holes from accumulating in the channel and lower layers, thus eliminating the PBE.

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Corresponding author. E-mail: ammar.sleiman@uniroma2.it

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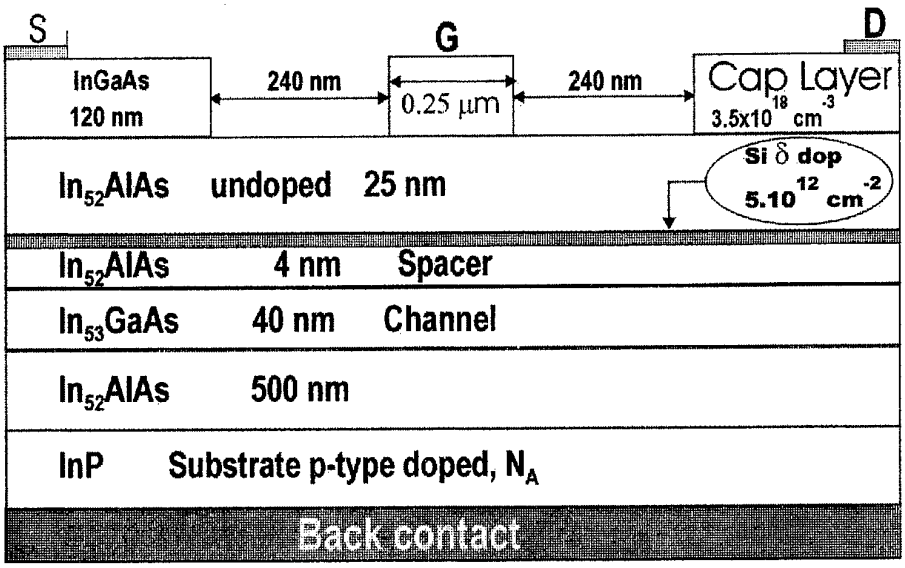


**Figure 1.** Schematic cross-section of the lattice matched HEMT with body contact (BC). The BC is formed by a highly p-type doped substrate connected to an ohmic back contact.

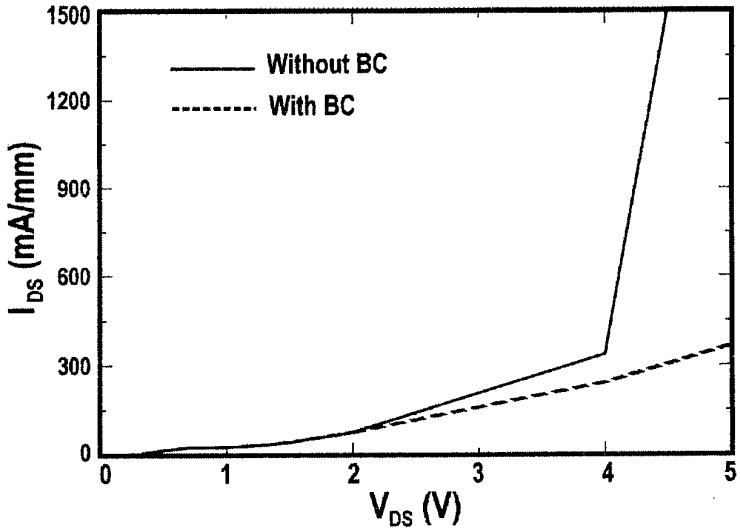


**Figure 2.** Simulated InP-LM-HEMT characteristics obtained in off-state condition ($V_{GS}$=-2.0V). Without BC (continuous line) the drain current goes directly to breakdown at $V_{DS}$=4 V. With BC (dashed line), the breakdown voltage is shifted from 4V to 5V.

**The significant differences of $Al_2O_3$ (0001) substrate nitridation by a nitrogen radio frequency plasma source at high and low substrate temperatures**

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The sapphire nitridation is a very critical step in the epitaxial growth of GaN by all growth methods. The nitridation of the (0001) $Al_2O_3$ surface by a $N_2$ rf-plasma source (HD25 of O.A.R.) used in GaN Molecular Beam Epitaxy has been investigated. Our experiments aimed to clarify the effects of three parameters of the sapphire nitridation treatment: (1) the ex-situ chemical preparation of sapphire, (2) the substrate temperature during nitridation and (3) the intensity of the nitrogen plasma beam. Significant nitridation occurred during 100min at a high temperature (HT), in the range of 550-800°C, and the nitridated layers usually exhibited three-dimensional islands, while weak nitridation occurred at a low temperature (LT) of 150°C and resulted to atomically flat surfaces. Linear time dependence has been found for the HT nitridation and the nitridated sapphire thickness extended to a region of approximately 1.5 nm, according to high resolution electron microscopy (HREM) observations. However, a higher strain relaxation was generally observed (by RHEED) for LT nitridation, although in one case no relaxation was observed. Sapphire etching in a HF solution (before substrate nitridation) created oxygen vacancies and increased the nitridation effect of the high substrate temperature. Finally, the structure of the nitridated surface controlled the polarity of overgrown GaN layers when a GaN nucleation layer was used. High nitridation temperature resulted to Ga-face and low temperature to N-face polarities of overgrown GaN films. The N-face material exhibited very good crystalline quality, while high defect densities characterized the Ga-face GaN. HREM revealed the occurrence of cubic pockets near the GaN/$Al_2O_3$ interface for the N-face material. The N-face layers also exhibited higher photoluminescence intensities and shorter linewidths at 15K and 300K. An electron background concentration in the low $10^{16}$ $cm^{-3}$ range and mobility above 200 $cm^2$/V.sec were determined for the N-face material by 300K Hall effect measurements, while the Ga-face layers exhibited very high resistivity values.

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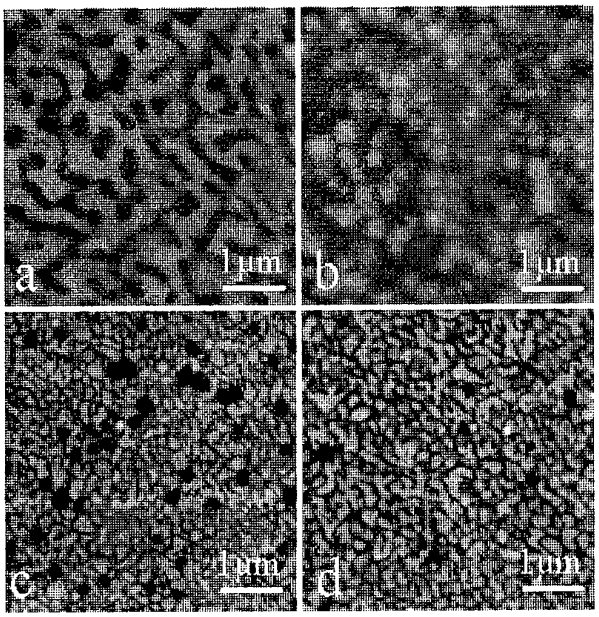


**Figure 1.** AFM photographs for (a) as-grown N-face GaN, (b) N-face GaN after etching in KOH solution, (c) as-grown Ga-face GaN, (d) Ga-face GaN after etching in KOH solution.

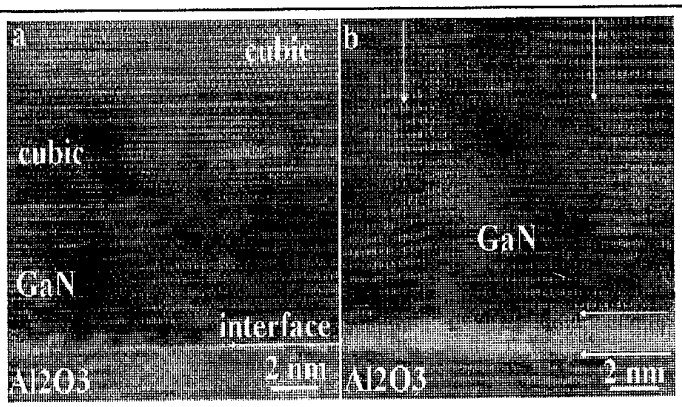


**Figure 2.** Cross-section HRTEM images viewed along <11-20> GaN axis. a) LT nitridation specimen: The sharp GaN/$Al_2O_3$ interface, depicted by the arrow, and "cubic pockets" in the GaN nucleation layer are shown. b) HT nitridation specimen: an extended interfacial zone (1.5nm) between GaN nucleation layer and substrate is visible. The arrows indicate IDBs bounding a domain of inversed polarity.

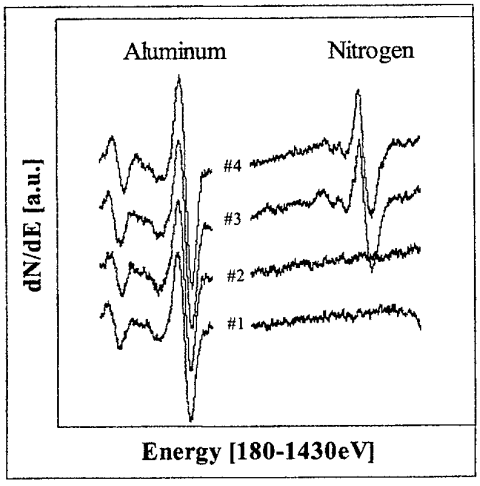


**Figure 3.** AES measurements on samples with high nitridation temperature (#3, #4) and with low nitridation temperature (#1,#2). Samples #1, #3 were etched in HF/$H_2O$ before nitridation experiment while #2, #4 were degreased using organic solvents. The N(KLL) peak was only observed for HT nitridation (samples #3, #4) and was more intense in the sample with HF/$H_2O$ preparation (sample #3).

# Low temperature-grown Be-doped GaAs for ultrafast optoelectronic applications

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Development of computing and telecommunications necessitates continuously increasing rates of data transmission. Future optical transmission systems, operating in the Tbit/s range, will require all-optical devices and optoelectronic devices with picosecond and subpicosecond response times. Besides, ultrafast semiconductor devices are also of interest for many other applications, such as emission and detection of THz radiation, triggering of high-speed electronics and characterization of high frequency microelectronics circuits. Implementation of ultrafast optoelectronic devices imposes requirements on materials from which the ultrafast optoelectronic components are fabricated. These requirements include: ultrashort carrier trapping and recombination times, high carrier mobility, high dark resistivity, good optical quality and high breakdown electrical field.

GaAs grown by molecular beam epitaxy at low temperature (LT) (200 – 300 °C) has been shown to meet these needs.[1] During the LT growth, about one percent of excess As is incorporated into the material. The excess As mainly forms antisite defects, $As_{Ga}$, situated in the middle of the band gap. Ionised antisite defects act as carrier trapping and recombination centres. A post growth annealing at high temperature (600 °C or more) induces precipitation of part of the excess As improving quality of the layers and making them semi-insulating. Further improvement of the LT-GaAs properties is achieved by doping the semiconductor with beryllium.[2] Beryllium, being a shallow acceptor in GaAs, ionises antisite defects and increases the number of active traps. Be incorporation also reduces the number of nonstoichiometry-related point defects in a LTG layer and improves its crystalline quality.

The goal of the LT-grown material engineering is to control the resistivity and the trapping time by a fine adjustment of defect compensation ratio. In the present work we make an attempt to find optimal parameters of Be-doped LTG GaAs by investigating carrier trapping and recombination over a wide Be-concentration and annealing temperature range. Here we should note that the carrier trapping time determines the response time of a device while the recombination time establishes the time in which the device returns to its initial state.

Carrier trapping times were measured by a time-resolved photoluminescence (PL) using up-conversion set-up, which is based on a self mode-locking Ti:sapphire laser (80 fs, 95 MHz, 780 nm). Electrons, photoexcited with a short laser pulse, are trapped to the ionised antisite defects at a rate which is much higher than the rate of the radiative recombination. The decay of the PL signal reflects the rate of the electron trapping.

Fig. 1 shows PL transients for Be-doped ($3\times10^{17}$ $cm^{-3}$) LT-GaAs samples annealed at different temperatures. The carrier trapping rate decreases with increasing anneal temperature demonstrating a decrease of the number of active electron traps because of As precipitation, which is more effective at high temperatures. The dependence of the electron trapping time on the anneal temperature becomes much weaker for higher Be concentrations (Fig. 2).

This can be understood taking into account that Be makes precipitation of excess As less efficient. The overall decrease of the trapping time with increased Be-doping is determined by a larger number of electron traps, activated by Be-doping.

The trapped electrons stay in the trapping levels until they recombine with a photoexcited hole. To monitor this hole trapping time, or recombination time, we performed a two-colour pump-probe experiment using an amplified Ti:sapphire laser system and two optical parametric generators. In the experiment, the pulse of 650 nm excites electrons from the valence band and the neutral traps into the conduction band. The photoexcited electrons are quickly captured to the trap levels. The probe pulse has a wavelength lower than the GaAs band gap, 1460 nm, and a much lower intensity. The changes in transmission of the probe pulse are determined by transitions of the trapped electrons into the conduction band. When the trapped electrons recombine with the photoexcited holes, the transmission for the probe pulse returns to its initial level. The decay time of the induced absorption provides the hole trapping time.

The dynamics of the induced absorption for a sample with $1.6\times10^{18}$ $cm^{-3}$ Be is shown on Fig. 3. The absorption decay time is 4.1 ps. A similar decay time of 5 ps is also observed for a sample with Be concentration of $2.5\times10^{17}$ cm-3. Though this value is larger than the electron trapping times, it shows that Be-doped LT-GaAs has a potential to be used in devices operating in a 100 GHz range.

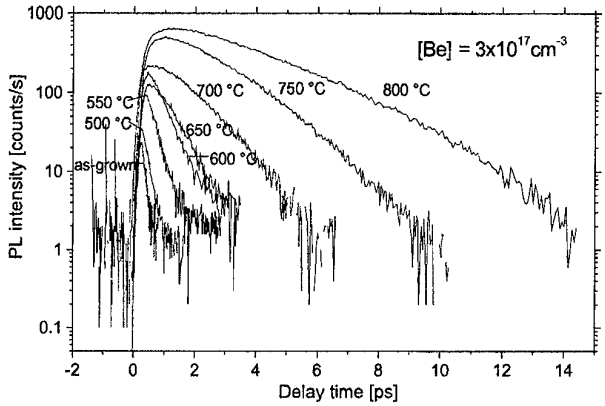


Fig. 1. Photoluminescence transients for the LT-GaAs Be-doped samples.

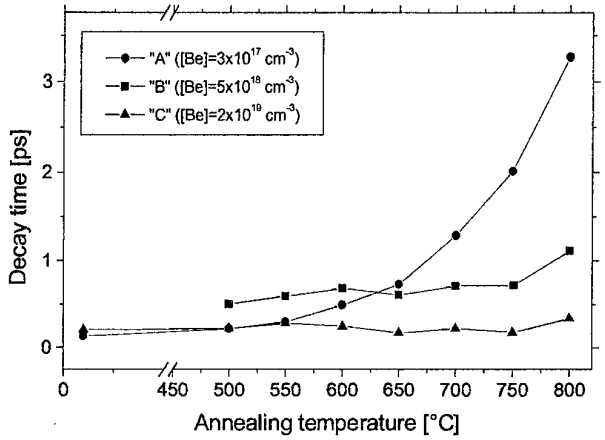


Fig. 2. Photoluminescence decay times for different Be concentrations and annealing temperatures.

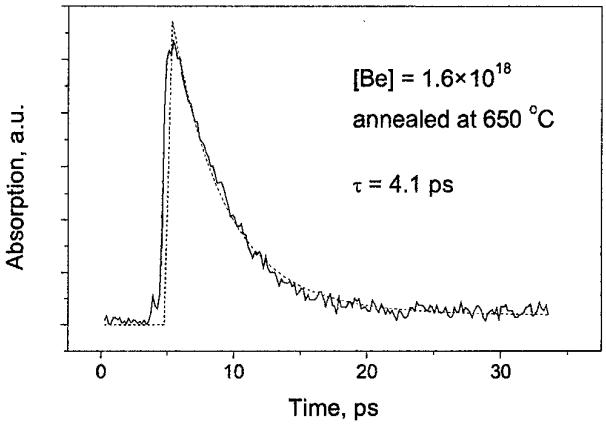


Fig. 3. Time-resolved absorption for LT-GaAs sample with $1.6\times10^{18}$ $cm^{-3}$ Be.


1. see for example S. Gupta *et al.*, IEEE J. Quantum Electron. 28, 2464 (1992).
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# Properties of InAs/GaAs lasers grown by MOCVD – application to ridge-waveguide geometry.

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*Index terms: semiconductor InAs/GaAs lasers, ridge-waveguide geometry*

## INTRODUCTION

In the recent work [1], we have reported on the investigation of InAs/GaAs monolayer quantum wells and short period superlattice (SPS) structures in the light of laser action. The experimental studies of oxide-insulated stripe geometry lasers have shown that the carrier collection is more efficient in SPS structure placed in the middle of the active region.

It is well known that the oxide-stripe geometry leads to the rapid increased in threshold current density as the stripe width is decreased due to lateral current spreading particularly when the sheet resistance of top cap and cladding layer is $\leq 2000\ \Omega$ [2]. To avoid this effect and to maintain lateral mode stability, it is important to confine the carriers and optical field in direction parallel to p-n junction plane. The above ideas are implemented in the ridge-waveguide geometry laser.

## FABRICATION

Our laser structures were grown by MOCVD on n-doped (001) oriented GaAs substrate. Lasers, as shown in the schematic in Fig. 1, consist of active region sandwiched between n-$Al_{0.35}Ga_{0.65}As$ Si doped 1300 nm thick and p-$Al_{0.35}Ga_{0.65}As$ Zn doped 550 nm thick cladding layers. To provide good electrical contact with the metallic electrode, a highly doped $p^+$-GaAs top capping layer 15 nm thick is used. The active region consisting of 9x1 ML InAs separated by 9x2.5 nm GaAs barrier layers and completed undoped GaAs ≈35 nm thick layers from both sides. The growth details of these structures are described in [1].

To produce ridge width of 5 μm, a standard photolithography and wet chemical etching is employed. Here, etching is stopped at ≈ 50-100 nm above the active region forming the ridge. Finally, the samples are cleaved into ≈ 290 μm length, and mounted substrate-side down onto base.

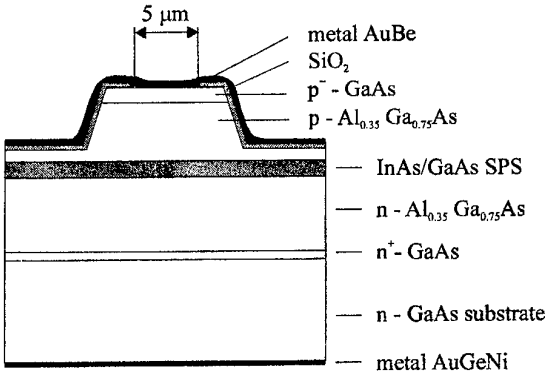


*Fig. 1. A cross-section of ridge-waveguide InAs/GaAs short-period superlattice laser.*

## EXPERIMENTAL RESULTS

All lasers are measured under pulse regime with duty-cycle 1% to avoid effects from excessive resistive heating. Samples are investigated in detail by performing the light versus current (L-I) characteristics, spectral characteristics and near-field pattern measurements.

Fig. 2 shows typical L-I characteristic of a 5 μm ridge width fabricated laser at room temperature. The threshold current is typically from 50 mA to 80 mA. It is clearly seen that the laser shows a linear dependence of the optical power output on the pumping current without kinks. This behaviour is believed to reflect a fundamental mode operation. It is confirmed by measurements of near-field intensity distributions at various pumping current levels as can be seen in Fig. 3. It is obvious that the near-field patterns are unchanged for various current operations.

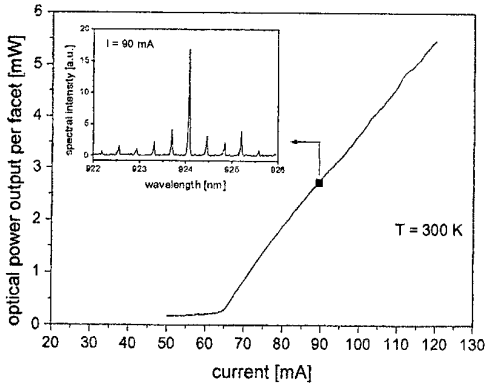


*Fig. 2. Pulsed light versus current (L-I) characteristic of a 5 μm width ridge-waveguide InAs/GaAs laser along with its spectrum measured at pumping current of 90 mA.*

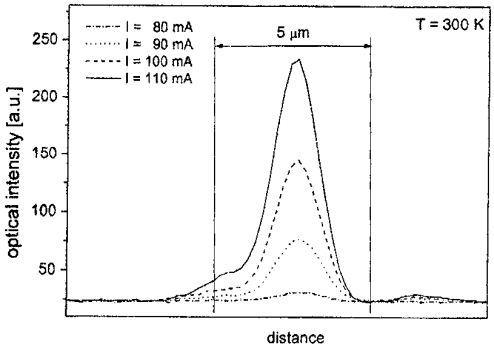


*Fig. 3. Near-field patterns of a 5 μm width ridge-waveguide InAs/GaAs laser for various pump currents.*

In view of longitudinal mode behaviour, lasers exhibit the multi-longitudinal mode structure as can be seen in connection with figure embedded into Fig. 2. The wavelength peak is observed at 924 nm. To determine a characteristic temperature $T_0$, the L-I characteristics of laser with a lower threshold current are measured at various temperatures. As a result, $T_0$ of 113 K is specified. Another examined operating characteristic is the external differential quantum efficiency that is 18.6 percent at room temperature.

## CONCLUSION

In summary, we fabricated the ridge-waveguide InAs/GaAs lasers having the ridge width of 5 μm. In comparison with the oxide-stripe geometry lasers so fabricated, the ridge-waveguide geometry lasers show the reduction of total threshold current density, as expected. In addition, stable zero-order mode up to about two times threshold is obtained.

## ACKNOWLEDGEMENT

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# Tunable Laser Diodes based on the Quantum Confined Stark Effect

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Wavelength-tunable laser diodes (LDs) are very much in demand in upcoming technologies such as optical telecommunications and optical interconnects. Recently [1], we proposed and presented a proof-of-principle demonstration of an optically pumped tunable laser device based on the quantum-confined Stark effect (QCSE). Such a device is compact, requires single current control, and can exhibit wavelength-switching times below 1ns. As a next step, we undertook the realisation of an electrically pumped LD device based on the same principle where appropriate band gap engineering intends to create a space charge field on the active quantum well (AQW) during lasing.

In Figure 1, we show a schematic band diagram of the active region we propose. It consists of three quantum wells (QWs) separated by two tunneling barriers. The central QW is the AQW one whose lowest transition is the ground state of the whole structure. The outer QWs are the collection QWs (CQWs), whose role is to collect the carriers that generate the space-charge field. To assure efficient carrier injection in the AQW it is essential to keep the barriers sufficiently thin to allow for carrier tunneling from the CQWs into the AQW. For electrical injection, the active region is incorporated in the intrinsic region of a p-i-n diode. The CQWs create a transient excess of electrons and holes on either side of the AQW, before the carriers end up by tunneling in the AQW to participate in the lasing. The resulting space-charge field acts on the AQW by the QCSE and tunes the emission wavelength $\lambda_L$ with increasing injection current, the space-charge field increases and $\lambda_L$ redshifts further.

InGaAs/AlGaAs triple quantum well structures have been grown on GaAs substrate by gas source molecular beam epitaxy with the triple quantum well at the centre of the intrinsic region of a p-i-n diode structure. The tunneling barriers and cladding consisted of $Al_{0.3}Ga_{0.7}As$, the CQW and AQW of $In_{0.1}Ga_{0.9}As$, and the separate confinement region of $Al_{0.2}Ga_{0.8}As$. This structure was processed in broad mesa of 75μm width and cavities of 1mm length were cleaved.

Shown in figure 2 are the edge-detected spectra recorded at 100K with increasing injected current density, between the lasing threshold 107A/cm$^2$ and 2667A/cm$^2$. To avoid heating effects, injection current is pulsed at 1kHz with pulse widths 5μs. We observe a clear redshift of $\lambda_L$ as the current is increased, that we attribute to the space-charge field created by a small fraction of the injected carriers. Red-shifts of $\lambda_L$ of up to 5nm in the 900nm spectral region have been recorded at this preliminary stage.

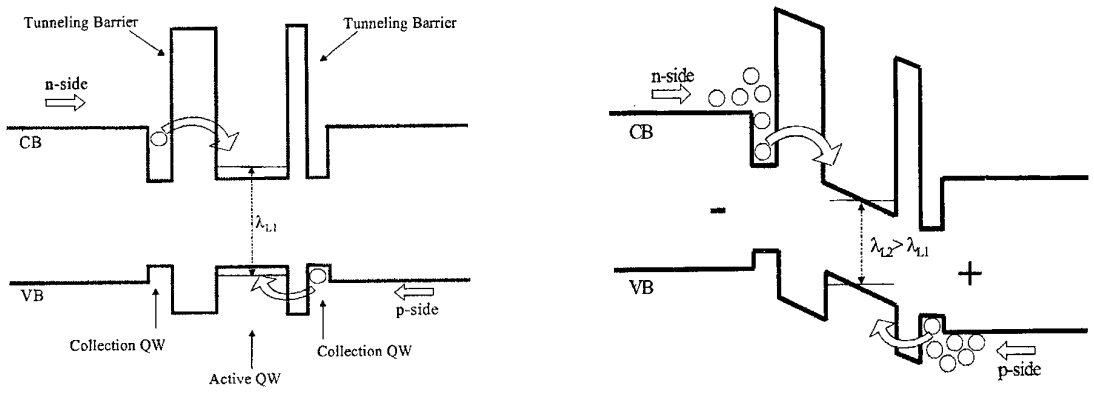


Figure 1: Schematic illustration of the energy-band diagram for the tunable QCSE laser diode, without and with electric field acting on the active quantum well.

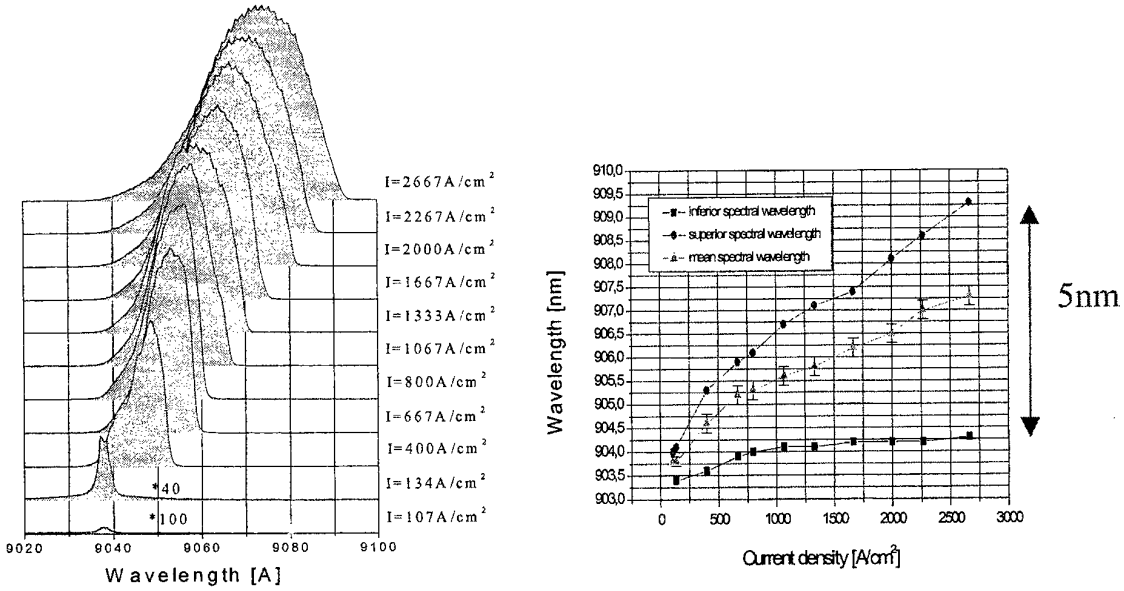


Figure 2: Edge emission spectra of the laser diode above threshold at 100K for various injected pulsed current density

## References

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# Current Collapse in GaN HEMTs

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*Abstract*— **Results related to electrical instabilities in AlGaN/GaN HEMTs will be presented. We have observed a large drain current and transconductance collapse, after the devices are biased in the dark at high $V_{DS}$; end-resistance measurements and measurements with inverted source and drain confirm that trapping occurs in the gate-drain access region, giving rise to an increase in the parasitic drain series resistance.**

## I. Introduction

GAN-BASED heterostructure field effect transistor are of great interest for high-power and high-frequency applications [1]. Although excellent electric characteristics have been achieved, the reproducibility and reliability of these devices are seriously affected by the presence of trapping phenomena [2,3,4].

AlGaN/GaN HEMTs tested (see fig. 1) were grown by MOCVD on sapphire substrate. These devices present a gate width of $150\mu m$, a gate-drain spacing of $0.5\mu m$, a gate-source spacing of $0.7\mu m$, and a gate length of $0.5\mu m$.

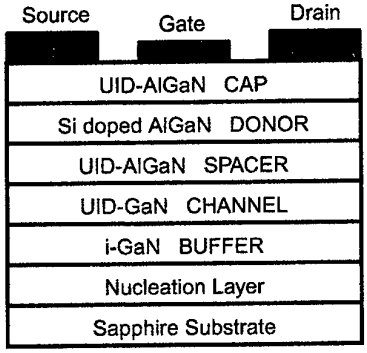


Fig. 1. Schematic cross-section of the tested GaN HEMTs.

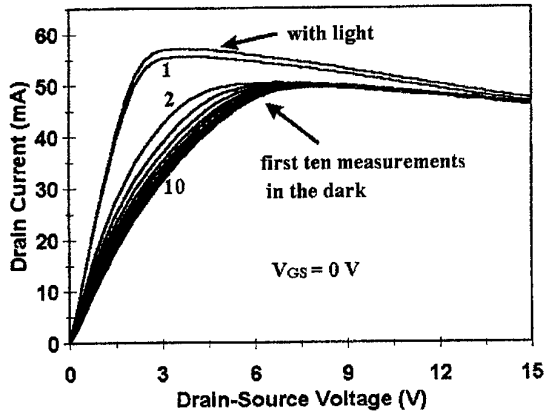


Fig. 2. Output characteristics ($V_{GS}$=0 V) with light and first ten measurements in the dark. Repeated measurements in the dark cause current collapse. The I-V characteristics present negative differential resistance due to self-heating.

## II. Current Collapse in Output Characteristics

Electrical instabilities related to a large drain current decrease have been observed in the tested devices. The drain "current collapse" takes place by keeping biased the device in saturation region, or simply by repeating test measurements. The collapse can be recovered by illuminating the device with white light. In figure 2, we consider the $I_D(V_{DS})$ measure up to 15 V with $V_{GS}$=0 V: the measure with light is followed by ten repeated measurements in the dark. A drain current reduction is observed suggesting the presence of trapping effects. The "current collapse" is observed only in linear region, while it is almost absent in saturation.

To explain this fact, we suppose that trapping phenomena takes place in the high-field gate-drain access region. Trapping of electrons in the surface cause an increase of the drain series resistance. Consequently at low $V_{DS}$ we note a decrease of the output characteristics slope, see Fig.3A . To confirm that the trapped charge is in the gate-drain access region, we measured the devices by swapping source and drain; in figure 3B are depicted the $I_S$ vs $V_{SD}$ characteristics before and after a stress (in the dark) at high $V_{DS}$. After the applied bias stress, the $I_S$ curve presents the current collapse both in the linear and saturation region.

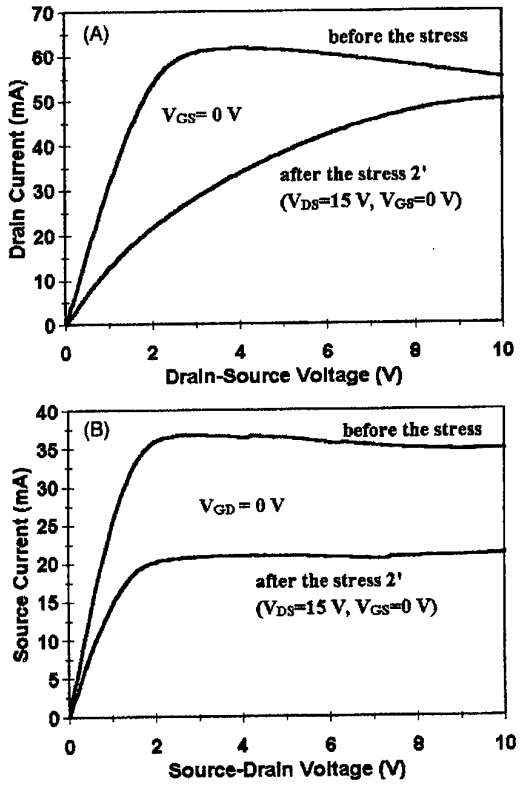


Fig. 3. (A) $I_D$ vs $V_{DS}$ with $V_{GS}$=0 V and (B) $I_S$ vs $V_{SD}$ with $V_{GD}$=0 V before and after the stress. Stress conditions: 2 minutes at $V_{GS} = 0V$, $V_{DS} = 15V$

## III. End-resistance, and trasconductance measurements

End-resistance measurements have been carried out before and after a bias-stress (in the dark) with high $V_{DS}$. The source resistance do not change after this test, while a large increase in the drain one takes place, see table I. This results supports the idea that trapping phenomena occurs in the gate-drain access region. Moreover, the illumination (3 minutes) after the stress detraps electrons and consequently the drain resistance recover the initial values.

TABLE I

DRAIN AND SOURCE END-RESISTANCE BEFORE, AFTER THE STRESS AND AFTER THE SUBSEQUENT ILLUMINATION (3 MINUTES). THE STRESS BIAS HAS $V_{DS}$=15 V, $V_{GS}$=0V, DURATION 2 MINUTES.

| | before the stress | after the stress | after illumination |
|---|---|---|---|
| $R_{DRAIN}(\Omega)$ | 21.4 | 52.1 | 23.7 |
| $R_{SOURCE}(\Omega)$ | 10.6 | 11.3 | 10.6 |

To gather more information, we carried out also measurements as a function of $V_{GS}$ at different device status. Figure 4 shows the $I_D$ and $g_m$ vs $V_{GS}$ characteristics before and after 1 minute of stress at $V_{DS} = 15V$, $V_{GS} = 0V$. A large decrease in both $I_D$ and $g_m$ is observed, furthermore it can also be noticed a slight threshold voltage shift. A subsequent illumination (3 minutes) allows the recovery of the initial electrical characteristics, as shown in Fig. 4 (the line *before stress* and *after stress and light (3')* are superimposed).

In Fig. 5 we note that $I_D$ and $g_m$ vs $V_{GS}$, with $V_{DS}$ in saturation region, do not exhibit any change after the applied bias-stress. The $I_D$ and $g_m$ collapse in linear region and the absence of collapse in saturation suggest that trapping effects give rise to an increase of the drain series resistance.

Figure 6 shows the normalized collapse of the $g_m$ peak value observed in different stress condition (filled symbols). After illumination a complete recovery can be observed (open symbol in fig. 6). The "collapse" increases with increasing $V_{DS}$ up to about $10V$, and after it saturate.

## IV. Conclusions

In conclusion, we have studied the "current collapse" observed in GaN-based HEMTs and it has been associated to the presence of trapping phenomena in the gate drain access region. This phenomena give rise to an increase in the parasitic drain series resistance, and to a decrease of the trasconductance peak values measured in the linear region. Finally, it has been observed that the "current collapse" can be completely recovered by illuminating the device by white light.

## V. Acknowledgments

This work was partially supported by MURST and PF CNR MADESS II.

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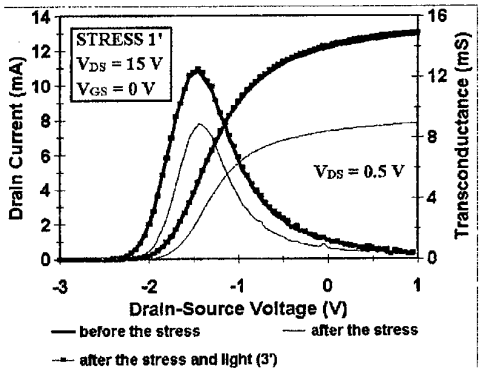


Fig. 4. $I_D$ vs $V_{GS}$ in linear region, after, before the stress and after the subsequent illumination: the first and the third curve are superimposed.

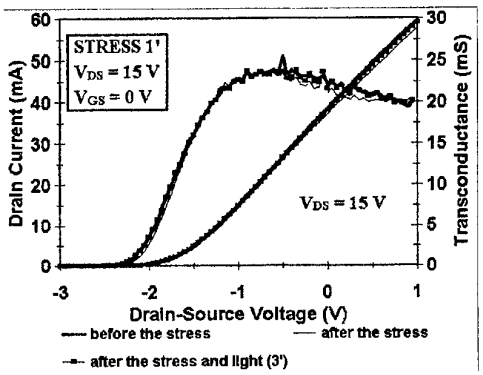


Fig. 5. $I_D$ vs $V_{GS}$ measure with $V_{DS}$=15 V, after, before the stress and after the subsequent illumination: after the stress the drain current and the transconductance do not exhibit any change. This confirm that the "current collapse" is negligible at high $V_{DS}$, when the device is in the saturation region.

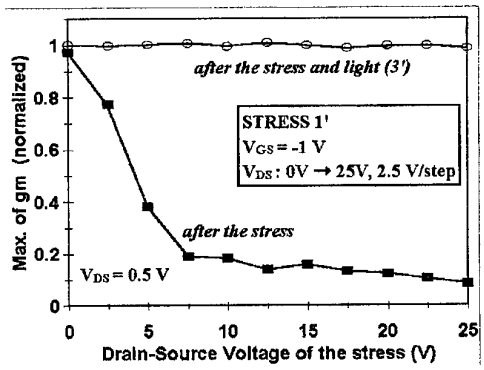


Fig. 6. Maximum of $g_m$ (with $V_{DS}$=0.5 V) after the stress and after the subsequent illumination, normalized to the value before the stress.

# Monte Carlo simulation of short channel MOSFETs in 3C, 4H, and 6H-SiC

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Silicon carbide (SiC) is a very interesting semiconductor material for high temperature, high frequency, and high power applications. The main reasons are its high saturation velocity, large thermal conductivity, high Schottky barriers, and high breakdown voltages

Short channel MOSFETs in 3C, 4H, and 6H-SiC are studied by using two-dimensional numerical simulations by the Monte Carlo method to investigate high frequency performances. Scattering mechanisms considered in our model are acoustic-deformation-potential scattering, polar optical phonon scattering, intervalley phonon scattering processes, ionized-impurity scattering and impact ionization. Our electron transport results (velocity-electric field characteristics, mobility) in 3C, 4H and 6H-SiC bulk materials compared to experimental data [1] and to Monte Carlo simulations in the literature [2, 3, 4] gives a good agreement.

The simulated structure sketched in figure 1, has a gate oxide thickness of 45 $A^{\circ}$, a junction depth of 0.1 μm. The source-drain extension [5] of length 0.1 μm have a Gaussien doping profile with maximum concentration at a projected range of 100 $A^{\circ}$, a parallel standard deviation and a transverse standard deviation range close to 800 $A^{\circ}$ and 400 $A^{\circ}$ respectively. The channel doping profile is also Gaussien. The doping level is $10^{19}$ $cm^{-3}$ for the heavily doped region. A uniform substrate doping concentration of $10^{16}$ $cm^{-3}$. For the surface scattering at the interface $SiC/SiO_2$, the electrons are scattered according to a specular model, where the normal component of the movement is reversed and the components parallel to the interface are maintained. In our model, we assume no charges on the oxide/semiconductor interface and in the oxide. We are using a coordinate system, where the y direction (figure 1) is parallel to the c-axis (4H and 6H-SiC).

For a gate length of 0.15 μm, the three ploytypes 3C, 4H and 6H-SiC are compared regarding transconductance $G_m$, cut-off frequency $F_c$. The simulated results are shown in figures 2 and 3. The drain-source voltage Vds is 5 V. The results (figure 3) of these calculations show that the maximum $F_c$ for 3C, 4H and 6H-SiC are 190 GHz, 175 GHz and 150 GHz respectively. The significantly lower Fc in 6H-SiC is a direct result of the lower electron mobility and to the higher anisotropy for this material

To get a comparison with silicon, we have made 2D Monte Carlo simulations in silicon for the same structure described above. The maximum cut-off frequencies versus gate length are plotted (figure 4) for Si and 3C-SiC. The drain-source voltage is 2 V for Si and 5 V for 3C-SiC. These results indicate that 3C-SiC MOSFETs could achieve better cut-off frequencies than Si MOSFETs ( a factor close to 1.5) with higher power densities. This is due to the higher saturation velocity ($2x10^5$ m/s) in 3C-SiC than in silicon ($1x10^5$ m/s). The simulation results show that SiC MOSFETs are very promising for high power and high frequency operations.

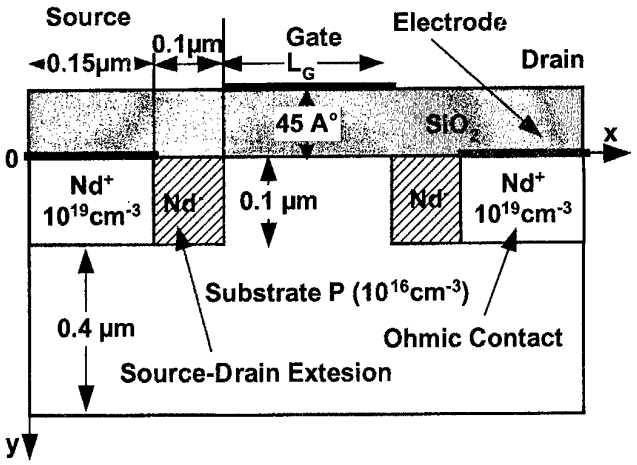


*Fig. 1: Schematic cross section showing simulated device structure.*

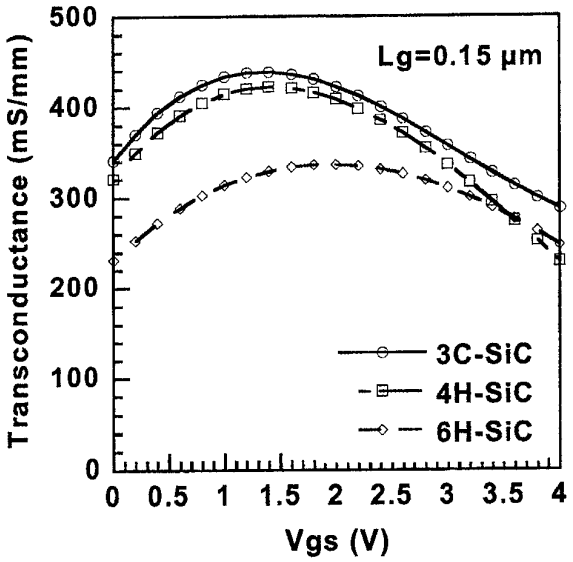


*Fig. 2 : Transconductance versus gate-source voltage for 3C, 4H and 6H-SiC MOSFETs. (Lg=0.15 μm, Vds=5 V).*

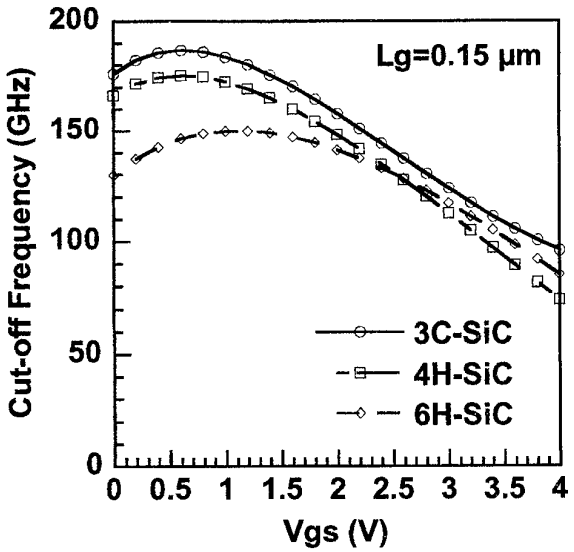


*Fig. 3 : Cut-off frequency versus gate-source voltage for 3C, 4H and 6H-SiC MOSFETs. (Lg=0.15 μm, Vds=5 V).*

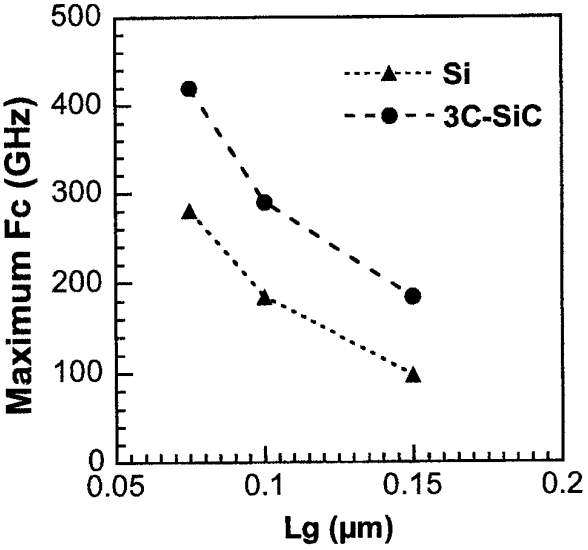


*Fig. 4 : Maximum Cut-off frequency versus gate length for 3C-SiC and Si MOSFETs.*

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# 60GHz 420mW/mm Low Gate Current GaInAs/InP Composite Channel HEMT on InP substrate.

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Power performances have been improved by studying different GaInAs/InP composite channel structure *(figure 1)* and by processing different drain extension devices. By using composite channel devices, we benefit from a better ionization threshold energy of the subchannel InP compared to the only GaInAs channel (1.69eV against 0.92eV). The difference of conduction band offset between the two materials ($\Delta E_C$=0.2eV) makes possible the electrons transfer from GaInAs to InP layer with the same electronic properties instead of increasing their energy and ionizing in GaInAs channel [1-5]. The main advantage is to reduce drastically the gate current issued from impact ionization. New process technology have been applied to compare these structures [6-7].

The components exhibit a drain current $I_{DS}$ of 750mA/mm at $V_{GS}$=+0V. The typical extrinsic transconductance is 600mA/mm. The Schottky characteristic in reverse gate to drain diode is –8V. The S-parameters are extracted from 1 to 40GHz. The cut-off frequency $F_T$ is 120GHz and the maximum oscillation frequency $F_{MAX}$ is 300GHz obtained with a 0.15µm gate length. Table 1 show sheet density carrier, mobility and square resistance of epitaxies The gate current resulting from the impact ionization phenomena *(figure 2 and figure 3)* was measured. It have been shown that the structure B and C present a better gate current issued from impact ionization. It is lower to 40µA at $V_{DS}$=4.5V *(figure 2)* for a large extension device which constitute the better result among the three structures. So, structures without second delta doping exhibit lower gate current. *Figure 3* show the gate current characteristic for three different drain extensions at $V_{DS}$=3V for the structure C. Similar behavior have been obtained with other epitaxies. At pinch-off, we show the current issued from tunneling effects. It is very small because we have a large diode breakdown voltage whereas at open channel, we see impact ionization current. In addition, the devices can not be biased over $V_{DS}$=5V without main risk of irreversible damage due to a large impact ionization in the channel. The lower impact ionization current for large extension implies that we have a decrease of electric field peaks which become spread into the structure. At low field, the GaInAs layer assume the conduction into the channel. At the exit of the gate at pinch-off and at the edge of the area recess beside drain where the electric fields are greater, the GaInAs and the InP undoped are depleted completely. A population of electron stay in the InP doped so that is the interest of this structure which allow to reach high values of $V_{DS}$ with a lower gate current and to obtain a great electron mobility in the channel and in access area. The devices have no kink phenomena in their characteristics due to the low impact ionization in the InP channel. Also, we improve power performances at 60GHz by reducing GaInAs channel and substitute the delta doping by a bulk doping. Large extension devices generated 306mW/mm (*structure A*), 422mW/mm (*structure B*) *(figure 4)* and 385mW/mm (*structure C*) at $V_{DS}$=3V and $V_{GS}$=-0.7V.

The structure and the topology play a significant role in term of performances optimization. Our results suggest that the extension of drain reduce the gate currents resulting from impact ionization and the structure optimization improves the power performances by improving carrier confinement in the channel. At 60GHz, we obtained (structure B) a maximum power of 422mW/mm, a 5.4dB gain linear, a 44% of drain efficiency and a 15% of PAE (*figure 4*) which constitutes the states of the art in term of output power at 60GHz.

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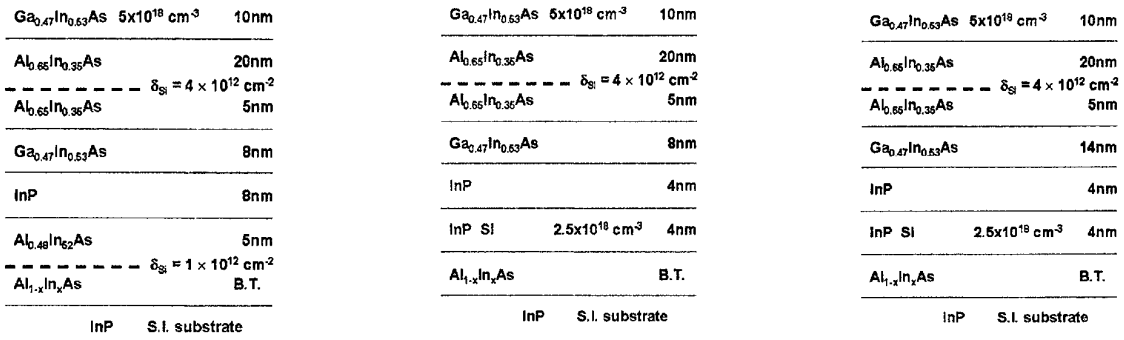


***Figure 1: Structure of the HEMT with composite channel on InP substrate***

| Epitaxy | $n_s(10^{12}.cm^{-2})$ | | $\mu_H(cm^2V^{-1}s^{-1})$ | | Square resistance(Ω) | |
|---|---|---|---|---|---|---|
| | 300K | 77K | 300K | 77K | 300K | 77K |
| A | 3.4 | 3.1 | 6350 | 13200 | 290 | 151 |
| B | 3.7 | 3.2 | 6950 | 16900 | 244 | 117 |
| C | 4.0 | 3.8 | 7120 | 20900 | 216 | 78 |

***Table 1: Sheet density carrier, mobility and square resistance of epitaxies***

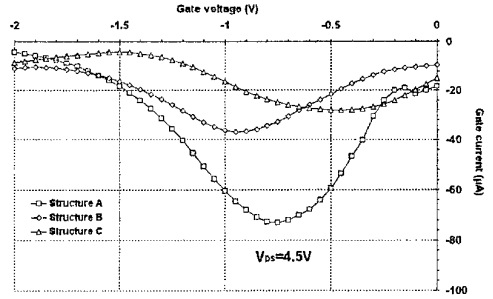


***Figure 2: Gate current characteristic of a large extension 0.15x100μm² Composite Channel HEMT at $V_{DS}$=4.5V for different structures.***

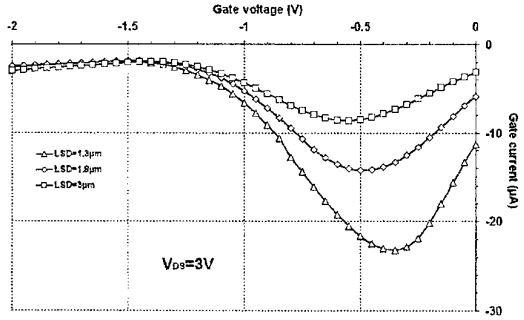


***Figure 3 : Gate current characteristic of a 0.15x100μm² Composite Channel HEMT at $V_{DS}$=4.5V for different structures***

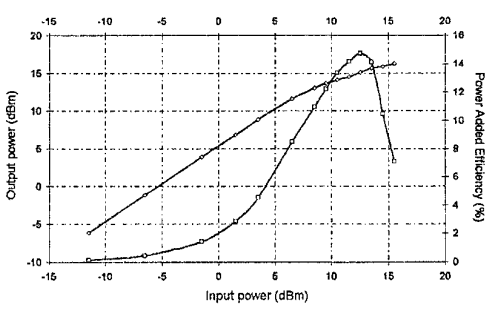


***Figure 4: $P_{out}$-$P_{in}$ and PAE at 60GHz of a 100x0.15μm² Composite Channel HEMT ($V_{DS}$=3V and $V_{GS}$=-0.7V)***

# SESSION VI
# Optoelectronics I
# Chair: Prof. Massimo Vanzi
# Tuesday May 29, 2001

| | |
|---|---|
| **8.30 am**<br><br>**INVITED** | **New frontiers of Quantum Cascade devices: towards a THz laser**<br>*A.Tredicucci[(a)], R. Köhler[(a)] R. Colombelli[(b)], F. Capasso[(b)], C. Gmachl[(b)], M. C. Wanke[(b)], A. L. Hutchinson[(b)], D. L. Sivco[(b)], and A. Y. Cho[(b)]*<br>(a) Scuola Normale Superiore and INFM, Piazza dei Cavalieri 7, I-56126 Pisa (Italy)<br>(b) Bell Laboratories, Lucent Technologies, 600 Mountain Avenue, Murray Hill, NJ 07974 (USA) |
| **8.55 am** | **Hot Electron Injection Laser: The Internal Base Potential**<br>*R.C.P. Hoskens, T.G. van de Roer, G.A. Acket*<br>TU/e Eindhoven University of Technology, Department of Electrical Engineering, Opto-Electronic Devices, EH8.16 Eindhoven, The Netherlands |
| **9.10 am** | **Development of MOVPE Strained Piezoelectric InGaAs/GaAs/AlGaAs Quantum- Well Double-Confinement Laser Structures on (111)A GaAs Substrates**<br>*J. Kim[(a)], S. Cho[(a)], A. Sanz-Hervás[(a)], A. Majerfeld[(a)] and B.W. Kim[(b)]*<br>(a) Department of Electrical and Computer Engineering, CB425, University of Colorado, Boulder, CO 80309, U.S.A.<br>(c) Electronics and Telecommunications Research Institute, P.O. Box 106, Yusong, Taejon 305-600, Korea |
| **9.25 am** | **Failure Criteria for Optoelectronic Emitter Degradation**<br>*H.-C. Neitzert[(a)] and A. Carbone[(b)]*<br>(a) Università di Salerno, DIIIE, Fisciano, Italy,<br>(b) Politecnico di Torino, Dip. di Fisica, Torino, Italy |
| **9.40 am** | **Optically Matched Side-Illuminated Photodetector for 1.3μm and 1.55μm wavelength Use Suitable For Hybrid Platform Integration**<br>*J. Harari[(a)], L. Giraudet[(b)], V. Magnin[(a)], J. Decobert[(b)], D. Decoster[(a)]*<br>(a) Institut d'Electronique et de Microélectronique du Nord IEMN, Av. Poincaré, Villeneuve d'Ascq, France<br>(b) OPTO+, Groupement d'intérêt économique Alcatel Alsthom Recherche, Route de Nozay, Marcoussis, France |
| **9.55 am** | **Improved Ultra Fast All-optical Shift Register and it's application for Optical Fiber Communication**<br>*Bo Tian, Wim van Etten, Wim Beuwer*<br>Telecommunication Engineering Group University Twente, 7500 AE, Enschede, The Netherlands |
| **10.10 am** | **Analysis and Modeling of Distributed Amplifiers**<br>*E. A. Karagianni and. N. K. Uzunoglu*<br>Microwave and Fiber Optics Laboratory, Electroscience Division, Electrical and Computer Engineering, NTUA |

# New frontiers of Quantum Cascade devices: towards a THz laser

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**Abstract:** despite the surging interest for a variety of applications involving wireless communications, medical and security screening, etc., the range of frequencies 1-10 THz is still characterized by a critical lack of compact, field-portable solid-state sources. However, semiconductor devices operating on transitions between confined states of the conduction band are making important steps in this direction. A new breed of quantum cascade lasers have been operated down to a frequency of 12.5 THz (24 μm) with continuous wave emission achievable at $\lambda \sim 19$ μm. Powers of few mW are obtained at liquid nitrogen temperatures. Active region design concepts and waveguide solutions here adopted provide useful insights in the important issues for performance improvement and for future developments towards energies below the optical phonon resonance.

Quantum Cascade (QC) lasers have rapidly established themselves as tunable coherent sources in the mid-infrared (MIR) range of the electromagnetic spectrum [1]. High power pulsed and cw operation has been achieved in the two atmospheric windows (3-5 μm and 8-13 μm) [2]. Research has since expanded to new material systems, ultra high-speed operation and mode locking, and the exploration of new frequency ranges [3]. The extension to the far-infrared range 1-10 THz is of particular interest and represents a very exciting challenge in today semiconductor physics and technology. At present, in fact, efficient, compact, solid-state sources for this spectral range, also known as the "terahertz gap", are still lacking, while the commercial interest is particularly high, thanks to the many applications in wireless communications, spectroscopy, medical and security screening. However, several fundamental physical issues and technological difficulties need to be answered in order for significant developments to take place. Increased accuracy in the band-structure design becomes one of the key factors to ensure high electron injection efficiency and to prevent hot-carrier effects. At these very long wavelengths, in proximity of the *reststrahlenband*, anomalies in the dielectric constant of the semiconductor complicate laser operation. Furthermore, free carrier absorption (increasing approximately with $\lambda^2$, $\lambda$ being the wavelength) becomes a dominating factor in the optical losses, while electron-electron scattering can no longer be ignored as a non-radiative relaxation channel. New types of waveguide concepts have to be adopted in order to reduce the otherwise prohibitive layer thickness, enhance the optical confinement and control the waveguide loss.

In this perspective, we discuss here the longest wavelength III-V semiconductor lasers ever reported, operating down to the lowest frequency of 12.5 THz ($\lambda \sim 24$ μm) [4]. They outperform in terms of output power any other semiconductor source of comparable wavelength, and laser action in continuous wave is also achieved up to $\lambda \sim 19$ μm with output powers in the mW range. The lasers are based on the QC scheme and rely on inter-miniband transition in so-called "chirped", i.e. appropriately graded, superlattices [5], which guarantee a large material gain even for low transition energies, close to the material forbidden *reststrahlenband*. They also employ a novel waveguide concept based on surface plasmons, TM electromagnetic modes confined at a metal-semiconductor interface. For wavelengths approaching the far infrared ($\lambda \geq 15$ μm), the penetration depth (skin depth) in the metal is largely reduced, so that a large mode confinement factor and low optical losses are obtained [6].
Low-temperature (8 K) emission spectra for two different lasers ($\lambda \sim 21.5$ μm and $\lambda \sim 24$ μm) are reported in Fig. 1. Under pulsed current excitation, the lasers oscillate on several longitudinal modes as typical of the Fabry-Perot resonators adopted. The highest peak powers (~ 40 mW at 10 K) are achieved at $\lambda \sim 17$ μm with approximately 3 mW for the $\lambda \sim 24$ μm device. Maximum operating temperatures are 240 K at 17 μm, 170 K at 19 μm, 140 K at 24 μm.

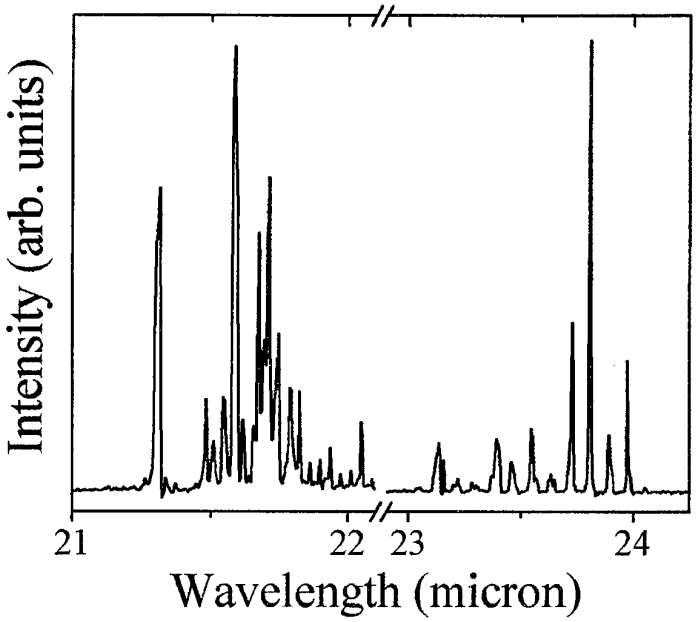


**Fig. 1** Pulsed (50 ns pulse width, 84 KHz repetition rate) emission spectra of sample D2691 (left panel) and sample D2696 (right panel). Devices are 36 μm wide and 750 μm long. The drive currents are 1.6 A and 1.75 A respectively. The spectra were measured in rapid scan using a Nicolet Fourier transform infrared spectrometer and a He-cooled Si-bolometer. The spectral resolution was set to 0.125 $cm^{-1}$.

The output power in continuous wave as a function of drive current is reported in Fig. 2 for a $\lambda \sim 19$ μm device, by far the longest wavelength ever reported for continuous wave III-V semiconductor lasers. Laser threshold was achieved at 370 mA (corresponding to a density $J_{th} = 3.2$ kA/$cm^2$), with the highest power (estimated to be around 1 mW per facet) at 460 mA. The emission takes place on a single longitudinal mode, with the non-monotonic behaviour of the light-current (L-I) characteristics correlating with mode hopping, as it can be seen from the inset. The device did not operate in cw above 10 K.

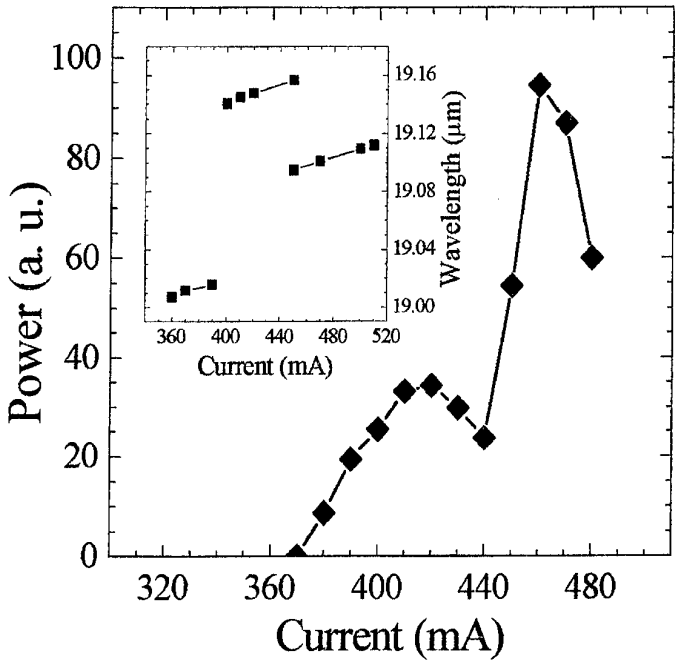


**Fig. 2** Output power as a function of continuous wave drive current at a temperature of 10 K for a $\lambda \sim 19$ μm Fabry-Perot laser device (375 μm long and 31 μm wide). It was recorded using a cooled HgCdTe detector, and the estimated power is of the order of 1 mW. In the inset the observed emission wavelength is reported for the various drive currents.

Complete and continuous single-mode operation over the whole current range is also achieved (for the case of pulsed excitation too) thanks to the adoption of a dual-metal Bragg grating which modulates the skin depth of the surface plasmon in a distributed feedback resonator.
Preliminary results have been obtained for QC light-emitting devices operating at ~ 3.5 THz. Spontaneous emission data and theoretical calculations show promising possibilities for future developments towards a THz coherent source.

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# Hot Electron Injection Laser: The Internal Base Potential

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***Abstract:*** *The Hot Electron Injection Laser (HEL), a three-terminal vertically integrated transistor-laser structure, is designed to investigate and possibly utilise carrier-heating effects on the optical gain and wavelength chirp. Simulations show the potential of carrier heating assisted gain switching to directly modulate the optical field intensity at frequencies up to 100Ghz and to control the wavelength chirp. Second generation devices now show lasing at 70K. Bias-dependent spontaneous emission spectra at 70K also show independent control of the carrier temperature inside the active region by both the injection current (+100K) and the heating voltage (+40K). The relative influence of the heating voltage on the carrier temperature varies between devices. The large variation in the base contact resistance seems to be responsible for this. A uniformly lower base resistance is expected to result in higher carrier heating efficiencies.*

## Introduction

Improving the high-speed performance of semiconductor lasers becomes increasingly urgent due to the increasing demand for transmission capacity in optical fibre systems. The data transmission speed has to be increased and the stability of the optical wavelength has to be increased.

Recently, it has been recognized that the gain and refractive index in a lasing device are governed by the energy distribution of the electron-hole plasma (carrier temperature) as well as its density. The effects of the carrier temperature are being studied now, for example, through optical pump-probe experiments on semiconductor optical amplifiers [1] and on short cavity and vertical cavity surface emitting lasers [2].

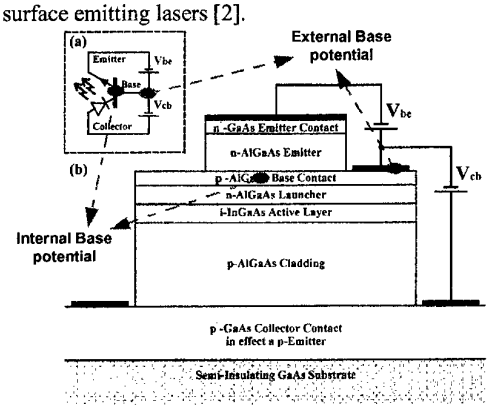


*Figure 1: Schematic design of the vertically integrated transistor-laser structure*

This project focuses on utilizing the carrier-heating effects to increase the modulation bandwidth while controlling the wavelength chirp [3]. Simulations show the potential of carrier heating assisted gain switching to directly modulate the optical field intensity at frequencies up to 100GHz and to control the wavelength chirp.

## Hot Electron Injection Mechanism

The carrier density and temperature affect the modal gain and index in an opposite manner and relax on different time-scales. The carrier energy distribution relaxes on a timescale of picoseconds while the carrier concentration typically relaxes on a timescale of nanoseconds. This phenomenon suggests the idea to enable high-speed modulation and controlled wavelength chirp by independently controlling the concentration and temperature of the injected carriers. This complementary modulation technique is implemented by means of a novel integrated transistor-laser structure [4]. The transistor region allows us to independently control the electron current injected into the laser region and thus the amount of carriers inside the active layer (AL) [Fig. 1: *Vbe*].

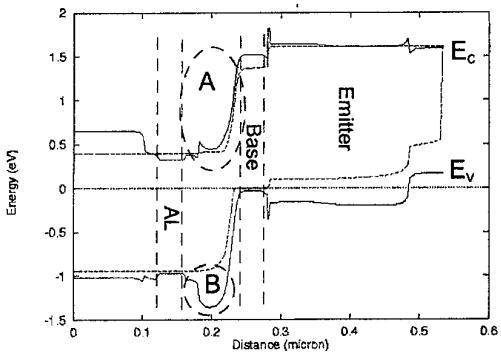


*Figure 2: Energy band diagram through the centre of the device. (A) Launcher's conduction band profile. (B) Launcher's valence band barrier*

Both regions are connected by the low-doped launcher, which takes up most of the voltage applied across the laser [Fig. 1: *Vcb*]. The resulting electric field heats up the electrons in a controlled manner before they enter the active layer [Fig. 2: *A*]. This enables the separate control of both the injected carrier current and energy.

## Internal base potential

The direct link between the external heating voltage Vcb and the internal voltage drop across the launcher [Fig. 2: *A*] determines, for a substantial amount, the carrier heating efficiency. Other factors influencing this efficiency are the launcher's conduction band profile, the launcher's material composition and various carrier-carrier interaction processes.

Lateral voltage drops in both base and collector layers have to be minimized accordingly. The base, as opposed to the collector, is located in narrow region with stringent design

rules. It requires a highly doped, narrow band-gap, material for proper bipolar operation but also confines about 5-10% of the optical mode. Minimizing the optical absorption means decreasing the doping level and increasing the band-gap. This trade-off might result in a base layer that is difficult to contact properly resulting in a lateral voltage drop for non-zero base currents. The internal voltage drop across the launcher will be lower and likewise the carrier heating efficiency [Fig. 3].

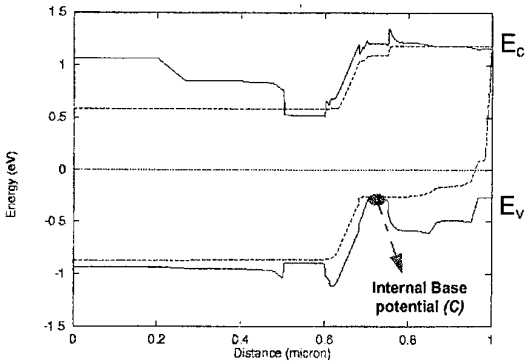


*Figure 3: Similar to figure 2, but with a non-zero base potential (C) due to a high base contact resistance [common base configuration]*

**Leakage currents across the launcher**

The first HEL devices showed high threshold currents, above 4kA/cm$^2$, due to high (radiative) recombination losses and intolerable high leakage currents [6]. The main source of leakage current is holes leaking out of the active region through the launcher and into the base [Fig. 2: *B*]. The heating voltage Vcb increases this leakage current by decreasing the valence band barrier between the active layer and launcher through the image force effect. Even though the effect is unwanted, it does show evidence of a proper, low-ohmic, base contact.

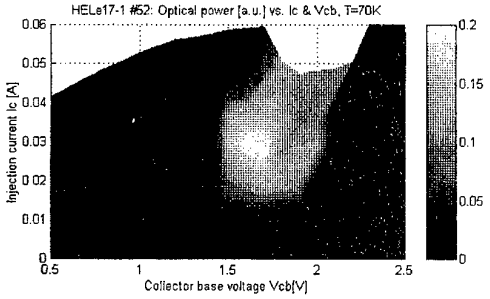


*Figure 4: Optical power vs. injection current Ic and heating voltage. [2nd generation HEL]*

**Lasing and carrier heating**

The second-generation devices showed a substantial decrease in hole leakage current. The InGaAs, instead of GaAs, bulk active layer and the n-type doping of the launcher increased the above-mentioned barrier effectively [7]. Decreasing the width of the Base/Launcher/AL region also decreased the radiative recombination losses inside the base and AL. Lasing is observed now at 70K, with threshold current densities of about 625A/cm$^2$ [Fig. 4].

These devices though show evidence of the above-mentioned problems resulting from a high base resistance. TLM measurements showed poor quality p-type contacts on top of the thin AlGaAs base layer. Further evidence is given by the electrical behaviour [Fig. 5].

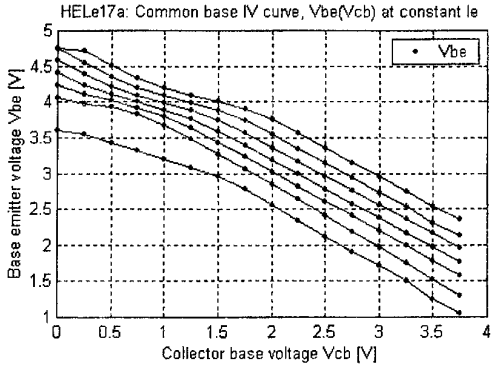


*Figure 5: Decrease in the required base-emitter voltage to keep the emitter current constant due to variations in the non-zero internal base potential [ΔVbe/ΔVcb≈1]*

Increasing the applied collector-base voltage decreases the required external base-emitter potential for a constant emitter current. The internal base-emitter voltage is pinned to the forward threshold voltage. Meaning the extra heating voltage drops completely across the base (contact) resistance.

These devices only show carrier heating due to variations of the electron injection current (+100K). The electron temperature is calculated from the slope of the high-energy tail of the spontaneous emission spectrum.

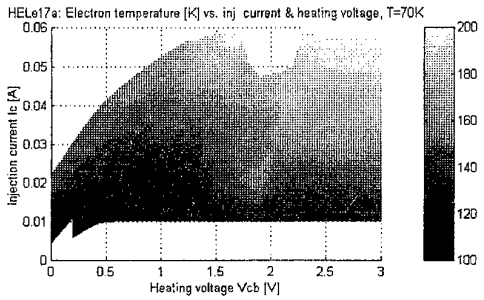


*Figure 6: Carrier heating vs. injection current and Vcb*

Devices having a slope ΔVbe/ΔVcb partly smaller than 1 do show carrier heating due to variations of the heating voltage (+40K). Currently the highest efficiency is around 30K/V, still below expected levels [5]. These devices switch on and off within a narrow band of heating voltages [Fig. 4]. Both electrical and optical behaviour are instable when lasing. Further work is necessary to explain these phenomena.

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**Development of MOVPE Strained Piezoelectric InGaAs/GaAs/AlGaAs Quantum-Well Double-Confinement Laser Structures on (111)A GaAs Substrates**

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There is an increasing interest in <111>-oriented strained Quantum Well (QW) structures on GaAs because they may lead to the development of novel or enhanced optoelectronic devices by exploiting the strain-induced Piezoelectric (PE) field [1] and the extended critical layer thickness [2]. There are also emerging results on the suppression of 3-D growth and the possibility of achieving atomically flat interfaces on the (111)A surface [3]. There are a few reports on strained PE InGaAs QW laser structures grown by MBE on (111)B GaAs substrates [4]. However, regarding MOVPE grown strained PE structures on {111} polar surfaces until recently there were only a few reports showing initial optical characteristics of InGaAs/(Al,Ga)As single confinement heterostructures. We recently demonstrated the successful MOVPE growth of GaAs/AlGaAs and InGaAs/GaAs PE QW structures on (111)A GaAs substrates with excellent interfacial and optical properties [5,6].

In this report we present the MOVPE growth and extensive characterization of [111]A-oriented InGaAs/GaAs/AlGaAs Double Confinement Heterostructures (DCH) in an N-I-P configuration (P+ GaAs substrate) for application to devices exploiting the PE effect. Undoped InGaAs/GaAs SQW structures were embedded between N- and P-type AlGaAs layers with 30% of Al. The In contents and well widths of the QWs are 17–20% and 70–110Å, respectively. The structural and optical properties of the QW structures were analyzed by High Resolution X-ray Diffractometry (HRXRD) and Photoluminescence (PL) spectroscopy. The strained QW embedded in the N-I-P DCH structure shows excellent structural and interfacial properties. HRXRD analyses using both symmetric and asymmetric reflections show that the structures are of high crystalline quality and that the QW strained layers are pseudomorphic. Figure 1 shows a representative HRXRD measurement and a theoretical best-fit for an N-I-P DCH structure. The calculated curve fits well the experimental profile without the need to include macroscopic in-plane relaxation, which indicates that the InGaAs QW is pseudomorphic. A narrow PL FWHM of 8.8 meV was achieved at 12 K for a 100 Å QW with ~ 20% of In as shown in Fig. 2, which corresponds to an interfacial roughness of about ± 1 monolayer. Laser diodes with conventional stripe geometry were investigated. We will present the achievement of laser action in these DCH laser diodes. To our knowledge this is the first observation of stimulated optical emission from laser structures fabricated in the [111]A orientation.

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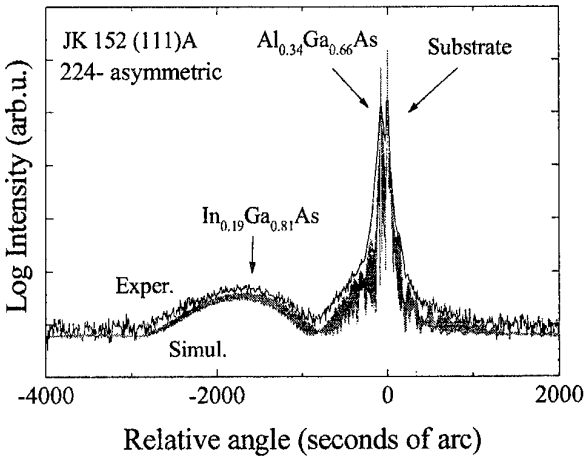


Fig. 1. The HRXRD profile and theoretical fit for a [111]A InGaAs/GaAs/AlGaAs N-I-P laser structure.

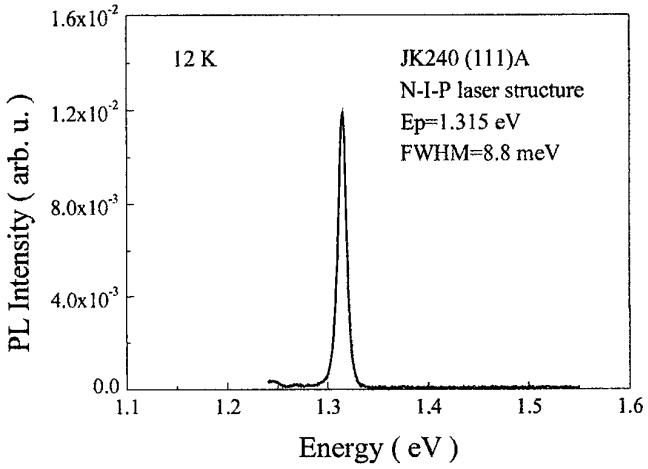


Fig. 2. 12 K PL spectrum of a [111]A InGaAs/GaAs/AlGaAs N-I-P laser structure.

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# FAILURE CRITERIA FOR OPTOELECTRONIC EMITTER DEGRADATION

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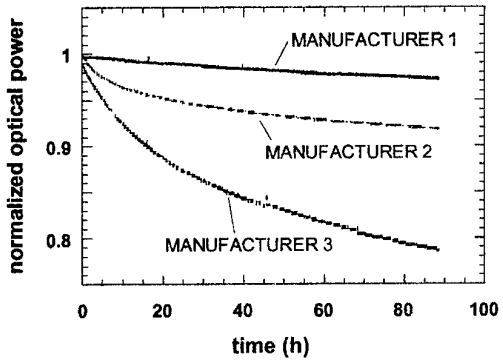
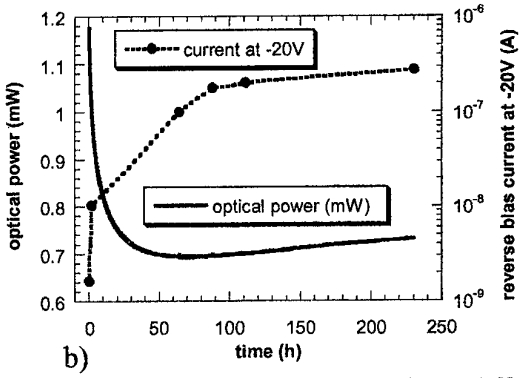
During aging studies of semiconductor lasers and light emitting diodes in general as a failure criterion for the degradation of these emitters a combination of a 3dB decrease of the optical emission for a given bias current and the increase of more than one order of magnitude of the current at a given bias voltage is adopted [1].For possible applications in fiber-optic house cabling systems [2] and in automotive optical bus systems the reliability of plastic optical fiber (POF) components is of interest. In Fig.1a we see the development of the normalized optical power of LEDs emitting at 650nm from three different manufacturers and observe even under moderate stressing conditions (constant current of 100mA applied at 25°C) already a considerable drop of the optical emitted power during the first 100h of operation. Further monitoring of the optical power and simultaneously of the reverse bias current at a given bias voltage (Fig.1b) of a LED from manufacturer 2, however, shows that in this case (at 70°C) already after 50h the degradation stops and subsequently the optical power is even slightly increasing. That means that the initial degradation - even if the dark current increasese for more than one order of magnitude - is not indicating a failing device but the missing burn-in process, often not suitable for low-cost devices. While in Fig.1b we find a correlation between electrical and optical data, this is not always the case.

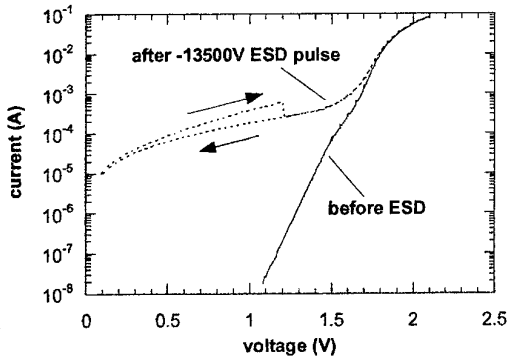



a)

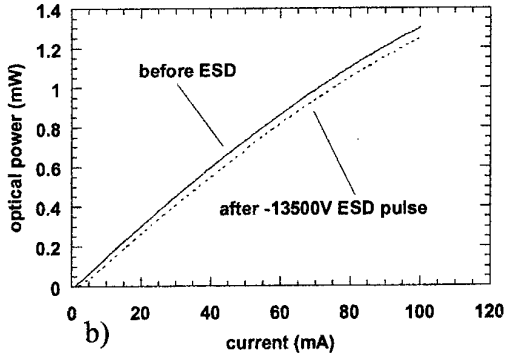



b)

Fig.1 a) Initial optical power decrease during aging at 25°C of 650nm emitting LED's from different manufacturers and monitoring of optical power and current of a LED from manufacturer 2 at 70°C




a)




b)

Fig.2 a) Current-voltage and b) Optical power-current characteristics of a LED emitting at 650nm before and after ESD induced degradation

In Fig.2 for the same type of device, measured before and after degradation of a negative bias human-body-model ESD pulse of -13500V we can see that extreme changes in the current-voltage

(I-V) characteristics - showing a largely enhanced forward bias current below 1.7V with a hysteresis due to charge carrier trapping after degradation - have almost no consequences for the optical power - current characteristics of the LED.

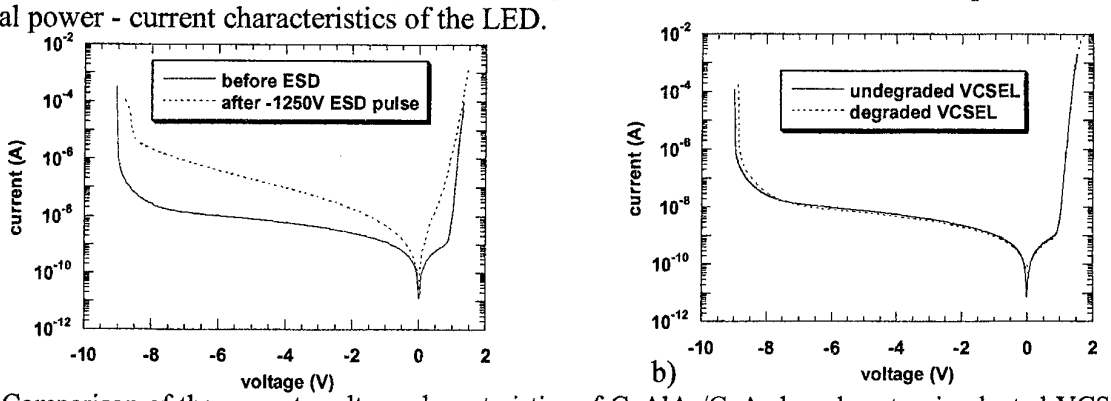



Fig.3 Comparison of the current -voltage characteristics of GaAlAs/GaAs based proton implanted VCSELs before and after degradation: a) due to constant current stress (3000h 20mA at 80°C) and b) due to ESD pulse stress with an pulse amplitude of -1250V

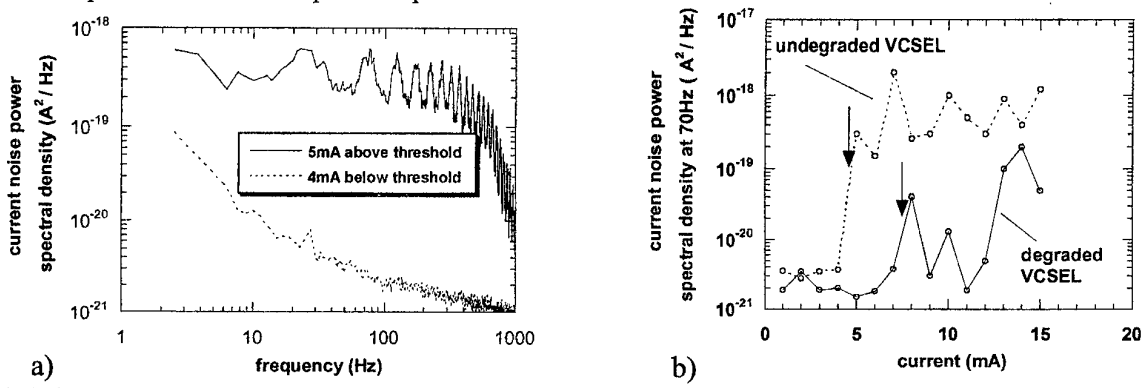



Fig.4 a) Current noise power spectrum of a GaAlAs/GaAs based VCSEL and b) current noise power spectral density at 70Hz as a function of the laser bias current of the device before and after constant current stress (as above). The VCSEL threshold currents before and after degradation are indicated by arrows.

In Fig.3a the current-voltage characteristics of a proton implanted GaAs/GaAlAs Vertical Cavity Surface Emitting Laser (VCSEL) before and after ESD induced degradation is shown. In this case the degradation resulted in a threshold current increase from 4.4mA to 5.3mA and the device degradation is well observed in the I-V characteristics by an increase of the ideality factor, an increase of the reverse bias current and a decrease of the reverse bias breakdown voltage.

After a constant current stress of the same type of VCSEL, resulting in a threshold current increase from 4.4mA to 7.8mA, we did not see any significant modification of the I-V characteristics (Fig.3b). In this case measurements of the noise power spectral density at low frequencies have been found to be a much more sensitive indicator of the device degradation, as already reported for optocouplers [3] and LEDs [4]. As shown in Fig.4a for the non degraded device, is the form of the noise power spectrum changing abruptly at laser threshold from a 1/f - type behaviour below to a lorentzian spectrum above threshold and the current noise power spectral density at 70Hz (Fig.4b) is increasing at the threshold for more than two orders of magnitude. In the case of the degraded VCSEL we see in Fig.4b the shift of the first increase of the current noise power spectral density at 70Hz to a higher current value and that the behaviour above threshold is not monotonic anymore.

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# OPTICALLY MATCHED SIDE-ILLUMINATED PHOTODETECTOR FOR 1.3μm AND 1.55μm WAVELENGTH SUITABLE FOR HYBRID PLATFORM INTEGRATION

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## Introduction

Since several years, the low cost integration of optoelectronic devices is a key problem for operators working in the field of optical telecommunications. The cost of optical device packaging, in particular the precise fiber pigtailing, was not critical when the optical links were used only in long haul telecommunication systems, because this cost was supported by all the network users. But as the fiber gets closer to the customer, the cost of optoelectronic devices is to be shared by a limited number of users. In this context, both laser and photodetector must follow low cost packaging scheme, and the silicon platform has demonstrated its interest by providing a precise alignment of a laser diode or a photodetector in front of a monomode optical fiber [1]. Considering the photodetector, it should be side-illuminated, with a large alignment tolerance, and should have a high responsivity. All these characteristics are difficult to get together since the usual epitaxial structure of side-illuminated photodetectors requires a lensed fiber to achieve an acceptable responsivity and consequently, the vertical alignment tolerance is small. For all these reasons, we studied an optically matched side illuminated photodetector for hybrid integration on silicon board.

## Design and Optimisation

The device, presented in Figure 1, is made of a GaInAs/GaInAsP/InP photodiode, evanescently coupled with a multimode optical waveguide. This waveguide is constituted of thin GaInAsP epilayers between InP layers. This particular structure leads to large optical modes allowing a very good coupling efficiency and a large vertical alignment tolerance when illuminated from a cleaved fiber [2]. The requirements governing our design and optimisation were :

- a high external quantum efficiency both at 1.3μm and 1.55μm wavelengths ( $\eta > 0.8$ )
- a small sensitivity to optical polarization ( ±0.2 dB)
- a high vertical alignment tolerance (better than 4μm).

The parameters to be found are the thicknesses of all epilayers, the length of the input waveguide and that of the photodetector active region. The optimization of the photodetector structure, defined by such a lot of parameters, has been carried out by using a genetic algorithm coupled to a Bidimensional Finite Difference Beam Propagation Method (2D-FD-BPM) [3]. As a result of this optimisation, the structure is optically matched to a cleaved fiber. The total calculated waveguide structure is 7.2μm thick and is based

on eight 0.1$\mu$m thick GaInAsP epilayers. The active region is 200$\mu$m long, with a 2$\mu$m thick low doped GaInAs absorbing layer. The GaInAsP N+ doped matching layer is 0.5$\mu$m thick and the input waveguide 50$\mu$m long.

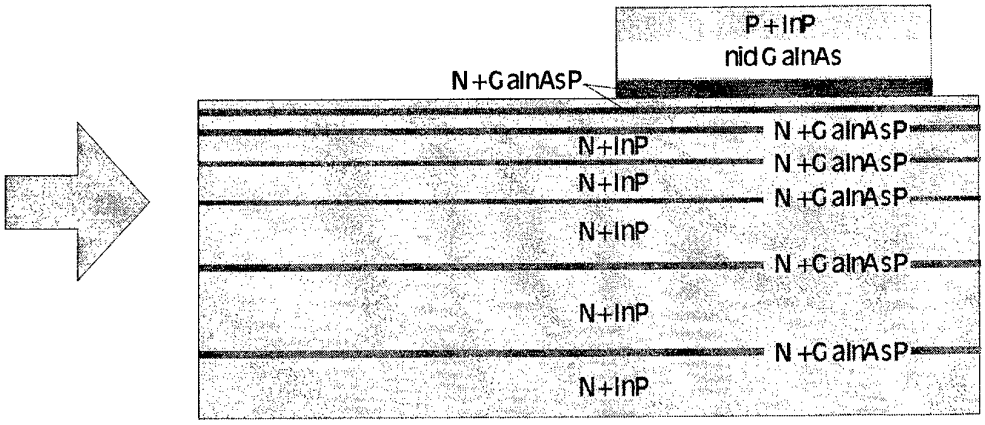


**Figure 1.** Typical structure of the Optically Matched Photodetector. In our case, we designed a waveguide with eight thin GaInAsP ($\lambda_g$=1.05$\mu$m) epilayers.

**Fabrication and Characterization**

The structure was grown by MOCVD and the photodiode was defined by mesa formation and P-type contact lift-off. The measurement set-up is made of an automated XYZ piezoelectric positioner to precisely align the cleaved fiber in front of the detector, and to measure the fiber position tolerances. The optical polarization is changed by using a simple Lefevre set-up. The performances are very high : the responsivities are respectively 1.05 A/W and 0.86 A/W at 1.55$\mu$m and 1.3$\mu$m wavelengths (quantum efficiencies equal to 0.85 and 0.86 respectively), the vertical alignment tolerances (at -1dB) exceed 6.5$\mu$m for both wavelengths and the sensitivity to optical polarization is lower than 0.1dB.

**Conclusion**

We have carried out the design, optimisation, fabrication and characterization of a new evanescent coupling photodetector suitable for hybrid platform integration. The results obtained are a high responsivity, a high alignment tolerance and a low sensitivity to optical polarization. Because of the great number of parameters to optimize, we used a genetic algorithm. All these results are promising and will be applied to get low cost high frequency photodetectors suitable for hybrid report on silicon platform.

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# Improved Ultra Fast All-optical Shift Register and it's application for All-optical Fast Packet Switch

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*Abstract: the improvements of an all-optical shift register beased on Self Electro-optic Effect Devices are presented. It can provide 8Gbps throughput for a 75μm long device. The ultra fast speed at 50Gbps is achievable with some improvements. Due to the convenience of operation in optical domain and electrical domain, it is very suitable for optical header processing; it is a candidate solution of IP over WDM.*

**Introduction**

In paper [1], an all-optical shift register was presented, this shift register can be operated in electrical domain as well as in optical domain. It is very suitable for optical header processing, and ideally can be used in fast photonic switching. Unfortunately since the implementation was based on a 326μm long device, the device capacitance limited the switching speed.

In this paper, several improvements are applied to the device both internally and externally. By using a short device (75μm long), the switching speed can be up to 50 Gbit/s. Considering the advantage of this device and the character of MPLS switching, an all-optical MPLS switch based in SEEDs is presented.

**Improvement of SEEDs**

The detail of the device physics can be found in [2]. A SEED's (Self Electro-optic Effect Devices) photo current-voltage characteristic for different waveguide lengths are shown in Figure 1. The input laser power is -6dBm at 1520nm; considering coupling losses of the waveguide, the estimation of the input power into the device of -12dBm is reasonable. A region of negative differential resistance was observed in waveguides as long as 326 μm or shorter. The size of the device should be optimized, if the size is too large, the device capacitance becomes larger, as a sequence, the switching speed is lower. On the other hand, if the device is too small, the absorption of photons will be more inefficient.

There are several ways to improve the switching speed of the S-SEEDs (Symmetric SEEDs): 1) By adding more quantum well layers, reducing the length of the device, the device capacitance will be decreased, however the photo current can stay at the same level.

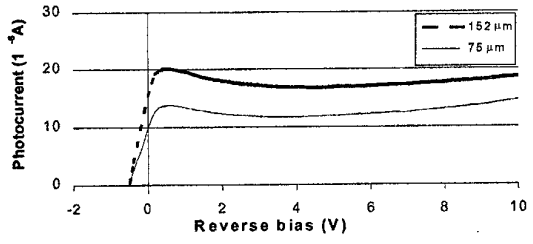


Figure 1 Photo current-voltage characteristic for different waveguide lengths

With the device 75μm long, the switching simulation was performed by applying an input data pulse of peak value of 1mW, initial value of 0.1mW, the referencing input power is keeping at 0.55mW constantly; the wavelength is 1520nm; the switching of S-SEEDs is shown in Figure 2. The switching time can be as short as 0.125ns, which means the S-SEEDs can operate at a speed of 8Gbps.

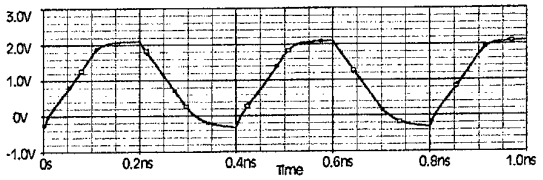


Figure 2 Switching voltage of S-SEEDs, the input pulse of peak value of 1mW, the wavelength is 1520nm

2) By integrating with external components as shown in Figure 3. An inductor compensates the device capacitance.

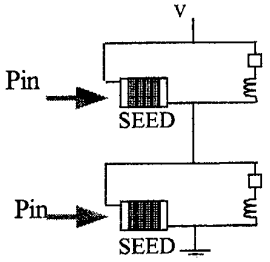


Figure 3 Improvement of SEED by using external intergated components

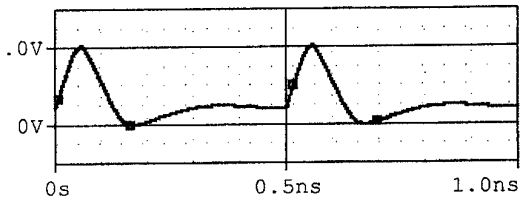


Figure 4 switching voltage of S-SEEDs with external resistor (12kΩ) and inductor (1μH)

From Figure 4, we can see by using a integrated inductor, the device switching speed can be up to 10Gbit/s

3) By using a pair of pump pulses before the data is injected into the device.

This operation uses a state-preset pulse operating at wavelength several nanometers longer than the SEEDs working wavelength. When the working wavelength is increased, the current peak will shift to higher voltage [2]. At the longer wavelength, the I-V curves tilt inward as shown in Figure 5 resulting in a single point of intersection. If the power of the state-preset pulse is much greater than

the input signal P1 and P2, and the state-preset pulse is equally applied to the set and reset windows, the SEEDs will be at the unstable state until the state-preset pulse is removed. After that any difference between $P_{in}1$ and $P_{in}2$ will unambiguously determine the state of the S-SEED. This operation reinitializes the device before each inputs to set the state of S-SEED, while allowing the clock and input signal to operate at the desired wavelength. The order of operation is state-preset pulse initializes the S-SEEDs at the unstable point: $P_{in}1$ and $P_{in}2$ values determine the S-SEED: and clock pulses read out the S-SEED states. The switching timing is showed in Figure 6.

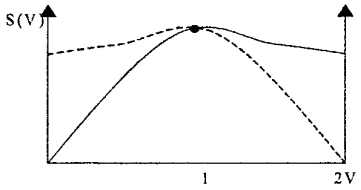


Figure 5 I-V switching characters of SEEDs at longer wavelength

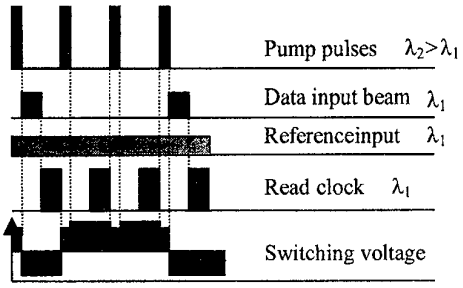


Figure 6 Switching timing of S-SEEDs with set-preset beams

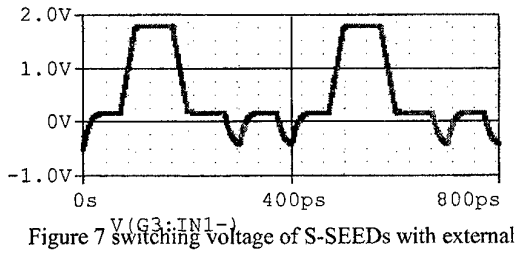


Figure 7 switching voltage of S-SEEDs with external 800μW pump pulses

The switching time can be shortened to 30ps as follows from Figure 7, which means the speed of 33 Gbit/s is achievable.

4) If we combine the two methods, a better improvement can be seen in Figure 8, the switching speed can be up to 50Gbit/s.

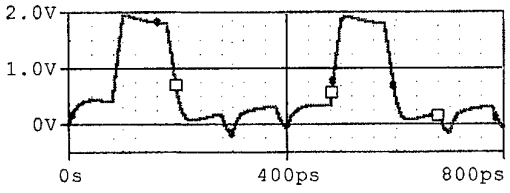


Figure 8 switching voltage of S-SEEDs with external resistor (12kΩ), inductor (1μH) and external 600μW pump pulses

**An all-optical MPLS switch based on SEEDs**

In Figure 9, an all-optical MPLS switch based on a SEEDs shift register is presented. An all-optical shift register constructed by using an S-SEEDs array is used to shift the IP packets. Optical connections (i.e. passive optical waveguides) are integrated between two neighbour memory cells. The clock signals of CLK and $\overline{CLK}$ can be generated by current modulating two laser diodes. After the two clock signals are coupled into the chip, they can be splitted by integrated beam splitters into CLK and $\overline{CLK}$ signals, which are connected to the odd memory cells and even memory cells respectively. "Data in" and "Ref" signals can be coupled into the first S-SEED optical window by a coupling system; the input signals and optical clock signals are coupled to the SEED windows by an effective waveguide coupler. A switch controller provides the clock synchronization, interface, label swapping, and network layer routing function by reading for LSRs (Label Switching Routers) and LERs (Label Edge Routers) and writing the all-optical shift register for LERs.

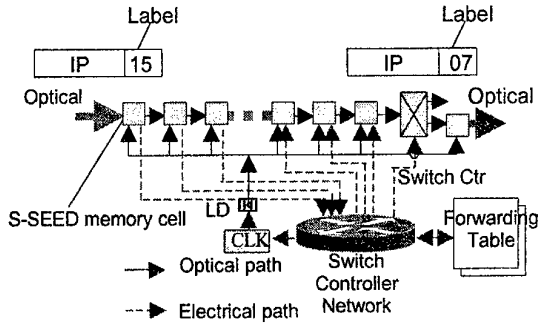


Figure 9 The implementation of all-optical MPLS switch based on SEEDs

**Conclusion**

In this paper, we proposed three methods to improve the switching speed of an all-optical shift register based on SEEDs, which can be used to implement an all-optical fast packet switch, optical wavelength convertor, optical modulator and optical memory. With combination of two improvements, the achievable speed of 50Gbps throughput is competitive for ultra fast optical communication systems.

Compared with other optical interconnection systems, the integrated scheme we present here, can replace the necessary mirror arrays, zoom lenses etc., and therefore it is easier to realize and more stable.

**Acknowledgement**

This work is part of the project "All-optical packet switch based on SEEDs". This project is supported by the Dutch Technology Foundation (STW).

**References**

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[2] H.G.Bukkems, et al. "An InGaAsP/InGaAs quantum well suitable for a Self Electro-Optic Effect Device", Proceeding of IEEE/LEOS Symposium Benelux Chapter, 1999, pp.243-246.

[3] Daniel O. Awduche, et al. "Multi-Protocol Lambda Switching: Combining MPLS Traffic Engineering Control With Optical Crossconnects", http://search.ietf.org/internet-drafts/draft-awduche-mpls-te-optical-02.txt.

# ANALYSIS AND MODELING OF DISTRIBUTED AMPLIFIERS

Dr. Evangelia A. Karagianni and Prof. Nikolaos K. Uzunoglu

*Microwave and Fiber Optics Laboratory,*
*Electroscience Division, Electrical and Computer Engineering, NTUA*
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The analysis and modeling of Distributed Amplifiers operating up to 40 GHz, in MMIC technology is examined. With a small-signal distributed model and traveling full-wave analysis based on T-parameters, an equivalent matrix which is consisted with linear scaling rules, is formed.

## *Formula for modeling two-port networks*

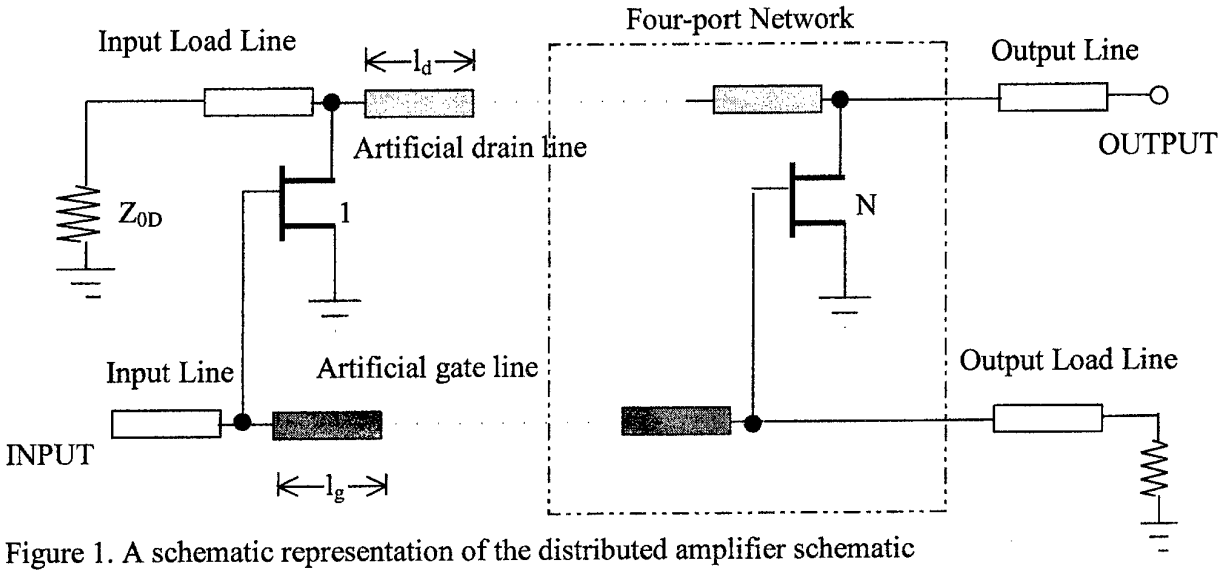
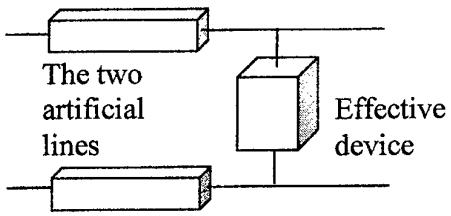



Figure 1. A schematic representation of the distributed amplifier schematic

Every two-port network can be modeled with its T-parameter matrix. So we consider, as it is shown in figure 1, the T matrix of the FET as well as the one of the artificial train line and the artificial gate line. Every stage of the distributed amplifier is concerned to be consisted of two lines and the effective device as we can see in figure 2.




The device we use is a H40 FET of GEC-Marconi Foundry with a 0.2 μm gate length. It operates up to 40 GHz. Taking into account the S-parameters for the range of frequencies DC – 40 GHz, with step one we exctract T-parameters using the following equations

$T_{11}=1/S_{21}$, $T_{12}=S_{22}/S_{21}$,

$T_{21}=S_{11}/S_{21}$, $T_{22}=(S_{12}S_{21}-S_{11}S_{22})/S_{21}$

Figure 2. The four-port network as it is applied in figure 1.

We do the same for the artificial gate and drain lines as well as for the load lines.

### *The Distributed amplifier as a two-port network*

Using figure 3, which gives 12 equations between $a_i$ and $b_i$ for i = 1 to 8, we solve the system for $(a_1,b_1, a_6,b_6)=A(a_3,b_3,a_8,b_8)$ where A is a 4x4 matrix which contains the T-parameters of the two-port networks. After all we form the N matrices for N cascaded networks and with a simple multiplication we form the T matrix. Terminating the four-port network with appropriate load lines, we can exctract a two-port network which is defined via T parameters. Changing these to S parameters we take a simple two port network modeled with S parameters in the frequency range DC to 40 GHz. We now can form the equivalent model for a 6 stages distributed amplifier and take the simulation of the two port network with the help of CAD tools (HP-ADS).

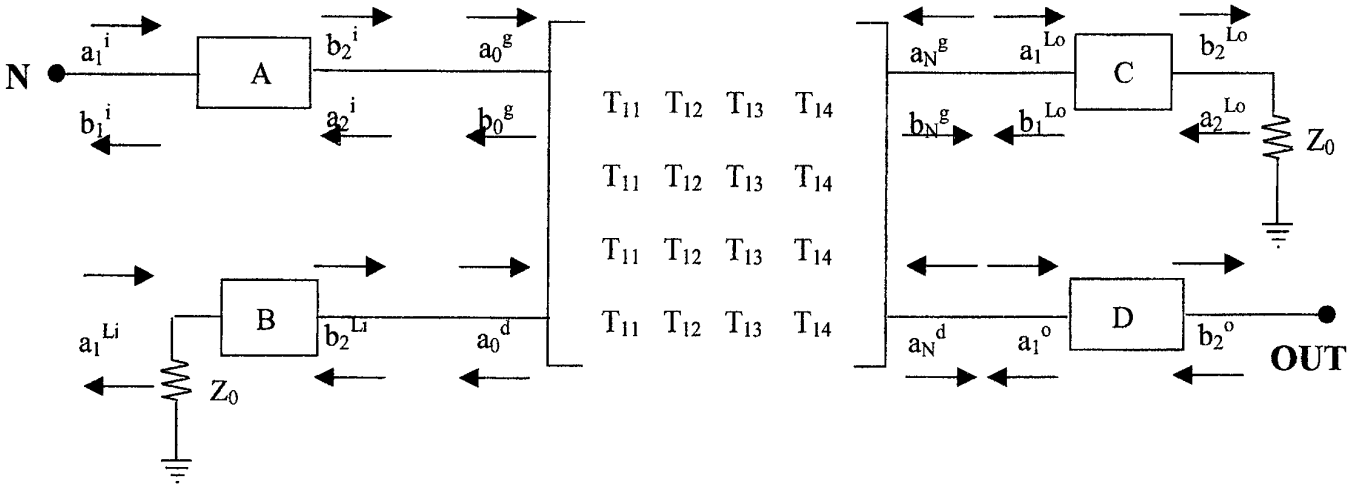



Figure 3. The T-matrix representing the four-port network

## *Comparison between mathematical analysis and simulation analysis*

The results, as sown in figure 4a are almost the same that arised from the simulation with the real components as it is shown in figure 4b. So, we find a new efficient tool in order to model linear FETs and transmission lines in order to be used as a CAD tool for linear analysis. Based on electromagnetic simulation and harmonic balance analysis, the proposed approach could be extended to nonlinear MMICs.

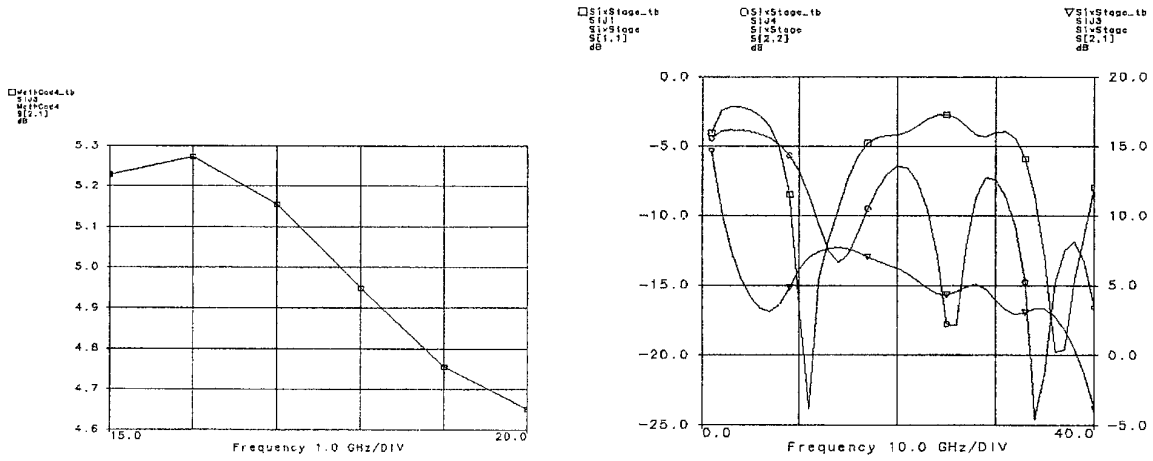



Figure 4. (a) Theoretical results (b) Simulation results

# SESSION VII
# Optoelectronics II
# Chair: Prof. Didier Lippens
# Tuesday May 29, 2001

| | |
|---|---|
| **10.50 am**<br><br>**INVITED** | **Development of InGaN on SiC LED and lasers at OSRAM**<br>*Volker Härle*<br>Osram Opto Semiconductors GmbH & Co. OHG |
| **11.15 am** | **Design and characterization of InGaAs/InP avalanche photodiode**<br>*F. Uherek, D. Haško and O. Lengyel*<br>Department of Microelectronics, Slovak University of Technology, Ilkovičova 3, Bratislava, Slovakia |
| **11.30 am** | **Optical Mode Transformers for Low Loss Coupling Between Fiber and InP-Based Photonic Circuits**<br>*K. Blary, B. Bellini, Y. Hernandez, J.F Larchanché, J. Harari, J.P. Vilcot, F. Mollot, D. Decoster*<br>Institut d'Electronique et de Micro-électronique du Nord I.E.M.N., av. Poincaré, Villeneuve d'Ascq, France |
| **11.45 am** | **Heterostrucure Solder Bumps for Optoelectronic Integration**<br>*C.G. Fonstad, Jr.,*<br>Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139, USA |
| **12.00 am** | **Performance optimization of GaAs-based terahertz photomixer**<br>*M. Mikulics[a, b], J. Darmo[a, b], D. Buca[a], A. Fox[a], M. Marso[a], A. Förster[a] and P. Kordos[a]*<br>(a) Inst. of Thin Films and Interfaces, Res. Centre Jülich, 52425 Jülich, Germany<br>(b) Max-Planck-Institute for Radioastronomy, D-53121 Bonn, Germany |
| **12.15 am** | **Comparison of Traveling-wave and Lumped-element 1.55 μm Photomixer for generation of THz radiation**<br>*M. N. Feiginov and V. Krozer*<br>Tech. University of Chemnitz, Reichenheiner Str. 70, Chemnitz 09107, Germany |

# GaN - Semiconductor material for future Lighting

V. Härle, D. Eisert, H.-J. Lugauer, M. Fehrer, S. Bader, B. Hahn,

J. Baur, U. Strauss

*OSRAM Opto Semiconductors, Wernerwerkstaße 2, D-93049 Regensburg, Germany*

During the last years GaInAlN became a material of extreme interest for both, research and industry, leading into various fields of applications in the UV-blue-green spectral region. As an example, blue LEDs are used in car dashboards or in LCD displays for backlighting. Other markets are signal applications and signs as well as communication. Due to long life times, low power consumption and low maintenance costs of such devices, LEDs are also very interesting for traffic lights. Here the research efforts are focused on the development of high brightness InGaN-LEDs with an emission wavelength of 505nm for the green signal light.
In order to address such markets, it is important to increase brightness of the single device. Therefor it is important to grow InGaN quantum wells with high Indium content and high quantum efficiencies on one hand. On the other hand the generated light needs to be extracted from the chip as well as from the LED-package.
Although the quantum efficiency of InGaN-LEDs is already comparably high, the dissipated heat in high power applications is still a major problem, so that heat management will become a major focus of development.
High brightness blue and green LEDs are also needed for active color mixing together with red LEDs in large area color displays. These displays can reproduce true color images with high quality even in a bright daylight environment.
Though all these applications have been important for the development of the Gallium Nitride technology, the real volume growth will start when the LED can enter the market of general lighting for illumination purposes. Electrical conversion efficiencies in the range of 10% are already comparable to that of incandescent bulbs, and in some time will match that of fluorescent lamps. Therefore LEDs have an important potential for energy saving. In addition their lifetime is much longer compared to that of conventional light sources, and the small dimensions of a LEDs allows completely new lamp designs.

Yet the requirements for illumination go far beyond the need of simply high optical power. First the main color needed for illumination is white. It is known that white can be mixed by a color with its complementary color, e.g. blue with yellow light. So blue LEDs are packaged together with a luminous converter that emits yellow light under irradiation with blue light. Yet this simple approach has several limitations:
On one hand it is just possible to reach a very limited part of the color table.
Therefore the deficiencies of such an LED in color rendering are clearly perceptible. Though the light emitted of such an LED looks white, human skin or plants illuminated with this LED-light look rather pale, because red and green parts are missing in the spectrum of the LED.
On the other hand the mixed color shifts when the emission wavelength of the exciting InGaN-LED changes due to variations in operating temperature and current.
These problems can be resolved by not using just one luminous converter, but two or better three. Then any color in between these converters can be composed by varying the relative concentration including a white LED with high color rendering index. Also the sensitivity to variations of ambient temperature or operating current are minimized.
The radiation of the LED is then only necessary for pumping of the converters. Therefore it is advantageous to use a short wavelength LED, because most converters can be excited efficiently by UV light.
When designing UV-LEDs, several requirements have to be taken into account:
The emission wavelength must be in a spectral range, where blue, green and red converters can be pumped efficiently. At the same time quantum efficiency has to be as high as possible for maximum light output and should not decrease significantly at increased operating temperatures, e.g. due to high driving currents.
Quantum efficiency decreases below 430 nm with shorter wavelengths due to the reduced density of localized energy states in the quantum well. At the same time the conversion efficiency increases at shorter wavelenghts.
An optimum regime is reached at an emission wavelength of about 400 nm. However the limitation of light output at high driving currents by thermal roll over still has to be overcome by improved heat management and an optimized design of the active zone.

# *Design and characterization of InGaAs/InP avalanche photodiode*

F. Uherek, D. Haško and O. Lengyel

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Ilkovičova 3, Bratislava, Slovakia
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*InGaAs/InP APD with separate absorption, charge and multiplication layer structure (SACM) has been designed, fabricated and characterised. In this design, the long-wavelength infrared light is absorbed in a narrow bandgap material ($In_{0.47}$ $Ga_{0.53}$ As), while the photogenerated carriers are transported to and multiplied in a wider bandgap (InP) material capable of sustaining high electric fields for avalanche gain without excessive dark currents from tunneling processes.*

*The base structure of designed InGaAs/InP SACM APD was grown in one epitaxial step by low-pressure MOCVD. A classical photolithography and wet chemical etching was used for mesa device processing. Measured current-voltage, capacitance-voltage, spectral characteristics and speed of response will be presented.*

## 1. INTRODUCTION

APD`s that operate at high bit rates and at the long wavelengths (1300 or 1500 nm) used in lightwave systems are inherently complex and costly to manufacture. At present, APD`s are therefore used mainly in long-haul networks predominantly at 2.5 Gb/s. Hi-Lo structures such as floating guard ring (FGR) APD [1], δ-doped APD, separated absorption, grading, charge and multiplication APD have been proposed for the very high gain-bandwidth (GB) product [2]. Recent studies of InGaAs/InP APD have been focused on a very thin multiplication layer.

In this work we report the design and results obtained from characterisation of InGaAs/InP based APD structures.

## 2. DESIGN AND FABRICATION

For optimum performance of high-sensitive receiver for fiber-optic lightwave systems operating at the 1300- and 1550-nm wavelength, the APD typically has a separate absorption and multiplication (SAM) layer structure. The doping and thickness of the epitaxial layers, particularly of the InP multiplication and charge layer, must be carefully controlled so that the electric field in the InGaAs absorber layer (referred to as the heterojunction field) is neither too high nor too low.

Designed structure of APD, as shown in Fig.1, is separate absorption, charge and multiplication (SACM) device, but uses a novel design. A designed layer structure consists of a 100 nm-thick InP buffer layer ($n \sim 3 \times 10^{17}$ cm$^{-3}$), a 2 μm-thick InGaAs absorption layer ($n \sim 1 \times 10^{15}$ cm$^{-3}$), 150 nm-thick InP charge layer ($n \sim 1.8 \times 10^{17}$ cm$^{-3}$) and a 500 (300) nm-thick undoped InP multiplication layer ($n \sim 10^{15}$ cm$^{-3}$). P-type 600 nm-thick layer ($p \sim 1 \times 10^{18}$ cm$^{-3}$) on the top of the structure is used as a contact layer. The entire InGaAs–InP APD structure is grown in single step by MOCVD. In this way, the junction position and the doping and thickness of the critical gain layer is precisely determined. Next, using wet chemical etching and standard photolithography, a shallow mesa is formed to define the lateral extent and thereby limit the capacitance and leakage current. The P and N contact layers are prepared by evaporation of Au-Zn and Au-Sn.

**MO 456**

| |
|---|
| InP ($p^+ \sim 10^{18}$) 600 nm - contact |
| InP ($\sim 10^{15}$) 500 nm - multiplication |
| InP ($n = 1{,}8 \times 10^{17}$) 150 nm - charge |
| $In_{0.53}Ga_{0.47}As$ ($\sim 10^{15}$) 2000 nm - absorption |
| InP ($n \sim 10^{17}$) 100 nm - buffer |
| InP <S> |

Fig.1 The cross-section of the SACM APD

## 3. DEVICE CHARACTERISATION

The current – voltage (I-V), capacitance – voltage (C-V), spectral characteristics and speed of response as the function of the voltage were measured and analysed. Fig.2 shows dark and photocurrent I-V curves of fabricated APD, with 0.023 $mm^2$ active area, using a focused 1310 nm laser-diode source. The breakdown voltage, $V_b$, was about 57 V and multiplication about 5. The responsivity at 10 V without antireflection coating was better then 0,75A/W at 1310 nm. From the C-V characteristic shown in the Fig.3 (including the capacitance of the package 0,9pF) one can see that the capacity is relatively low (lower then 1,1pF at operating voltage). The spectral characteristic at bias voltages higher than 10 V corresponds to the conventional InGaAs/InP PIN photodiode.

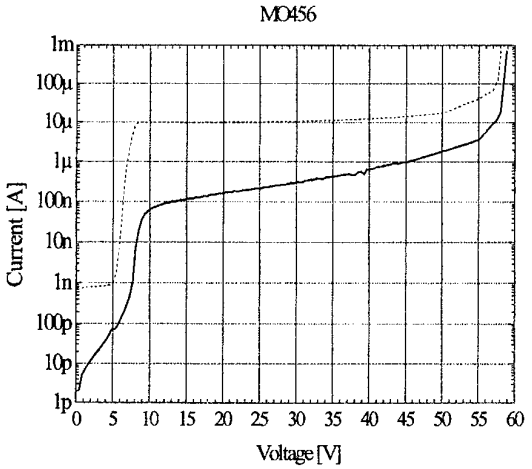


Fig.2 The I-V characteristics of MO456

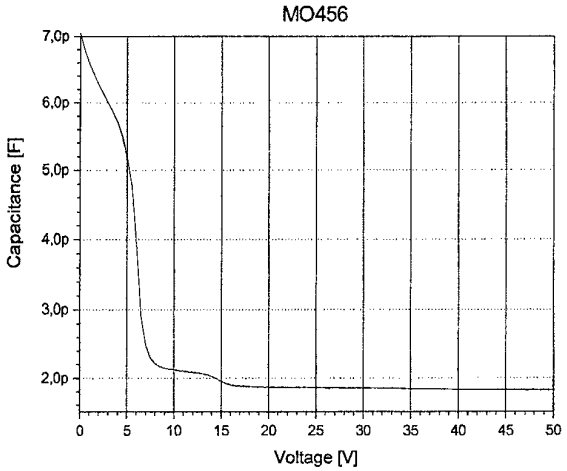


Fig.3 The C-V characteristics of MO456

For the time response measuring of SACM APD's 3GHz pulse generator HP 8133A and the high speed laser source BCP 51T/231 (1310 nm, 1.5Gbps) has been used to generate the optical pulses. Laser source generates an optical signal with optical power in the fiber 1mW. The rise and fall time has been measured using digital oscilloscope LeCroy 9326. The high-frequency response characteristics of photodiodes at the various gains are shown in the Fig. 4. The fast rise and fall component follows the relaxation oscillation of the InGaAs laser pulse and parasitic oscillation of photodiode header (it is about 0.9pF). The slow fall transient strongly depends on the bias voltage and is caused by pile-up effect on the heterointerface between absorption (InGaAs) and charge (InP) layer [x].

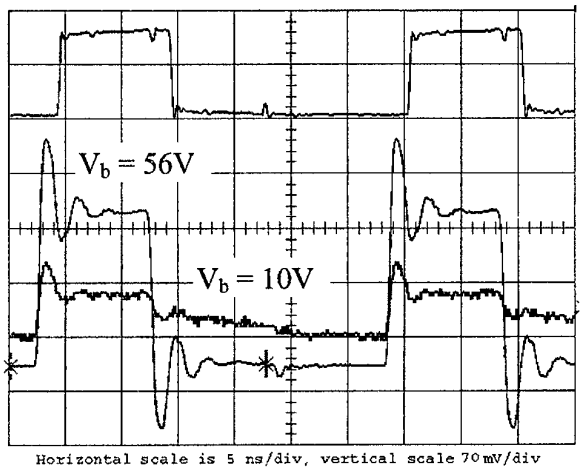


Fig.4 Time response of MO456 SACM APD at different reverse bias voltages $V_b$


### Acknowledgement

The work at the Microelectronics Department of Slovak University of Technology was supported by the project No.1/7600/20 and at the International Laser Center by the project No. 1/7253/20 and Slov/Nem/MLC all from Slovak Grant Agency.


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# OPTICAL MODE TRANSFORMERS FOR LOW LOSS COUPLING BETWEEN FIBER AND InP-BASED PHOTONIC CIRCUITS

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**J. Harari, J.P. Vilcot, F. Mollot, D. Decoster**

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## Introduction

Due to the increasing development of optical telecommunication systems, there is a strong need of low cost monolithic or hybrid photonic integrated circuits. In both cases, optoelectronic functions are realised by InP-based components. Yet the mode of an InP optical waveguide is significantly different from that of a standard fibre, and losses due to this mismatch still account for a lot in the global power budget. Hence the need for an optical mode transformer reproducible and easy to fabricate. The aim of this paper is to present the design, fabrication and characterisation of two parallel concepts of optical interconnection between fibre and typical InP/InGaAsP/InP optical waveguide of an integrated optics switching matrix. The first interconnection is a monolithic convertor made of thin quaternary epilayers distributed within InP. The second one exploits properties of preferentially etched silicon and of polymers.

## 1. Monolithic optical mode transformer

### 1.1. *Principles and design*

The optical mode of the InP/GaInAsP/InP waveguide is about 9 $\mu$m wide and 1.5 $\mu$m high. For this reason, an optical mode profile converters is necessary to improve the coupling efficiency with optical fibres and to maximise the misalignment tolerance. In the horizontal direction, insertion losses are decreased by enlarging the waveguide (cf. Fig. 1). In the vertical direction, the epitaxial structure of the converter, made of three thin quaternary epilayers distributed in InP, and located above the waveguide structure, is thicker and is matched to the circular mode of the fibre. The taper structure has been tested and optimised by using 2D and 3D-FD-BPM and a genetic algorithm. As typical optical behaviour of this multimode epitaxial structure, the optical beam propagates up and down periodically in the taper before being confined in the quaternary optical waveguide (cf. Fig. 2).

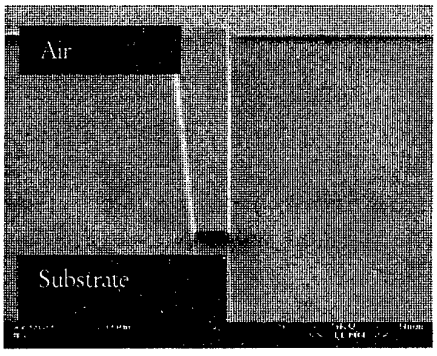


**Figure 1.** Photography of a monolithic taper

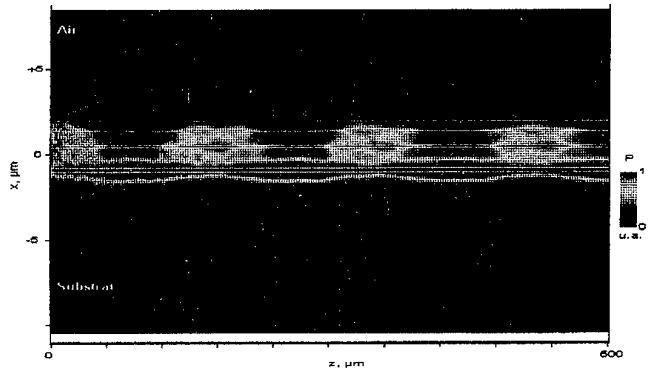


**Figure 2.** Light Propagation in the vertical plan (2D-BPM)

### 1.2. *Technology and measurements*

The epitaxial structure has been fabricated by MBE. The fabrication process is composed of three etching steps using a conventional e-beam lithography. $SiO_2$, deposited by PECVD, serves as a mask for the long etching of the tapers. A $CH_4/CHF_3$ Reactive Ion Etching process is used to etch $SiO_2$ and a $CH_4/Ar/H_2$ RIE process is used to etch the semiconductor materials. A thin AlInAs etch-stop layer introduced in the structure is used to control the etching depth. The device has been characterised at 1.55 $\mu$m wavelength with lensed and cleaved

monomode fibres. We first measured the near-field patterns from the output facets and performed then fibre-to-fibre measurements. Our results show coupling improvement better than 6 dB.

## 2. Hybrid optical mode transformer based on preferential etching of substrate

### 2.1. *Principles and design*

Anisotropic etching of crystalline substrate can lead to reproducible profile with strong geometrical properties. This is the case for InP (001) in a HBr aqueous solution and Si (100) in KOH aqueous solution. For instance, anisotropic etching of (100)-oriented Si produces U-grooves and stops itself when V-shaped grooves are obtained for which depth $d$ and width $w$ are linked according to : $d = w\frac{\tan(54.7°)}{2} = w\frac{\sqrt{2}}{2}$. Homothetic V-groove are thus obtained only by varying the width $w$, as shown on fig. 3. This is the base for a 3D taper: the optical spot, which is inscribed in V-shape, is controlled in both width and height with great precision. A transition between a fibre and an InP-based waveguide is designed as following. At the input, $w$ = 15 $\mu$m so that the overlap integral between the fundamental triangular mode and the fibre mode is greater than 0.9. Afterwards $w$ is decreased down to 5 $\mu$m within a length of 1 mm, and the overlap between this V-waveguide and a typical InP-based ridge waveguide is 0.86. In this case, 3D Finite Difference Beam Propagation Method shows additional loss due to transition of the order of 1 dB.

### 2.2. *Fabrication of the taper and measurements*

V-grooves fabrication is a classical semiconductor process. The second step concerns the proper filling of groove. We use BCB 3022-63 by Dow Chemicals, for its ability to planarise 15 $\mu$m-deep grooves (residual difference in height : $t$ = 0.1 $\mu$m for $w$ = 5$\mu$m). Polymer is then softly dry-etched (R.I.E. $O_2/SF_6$, 60 W) to substrate level. This step requires technological optimisation since the roughness of etched polymer surface will induce diffusion losses. Photography of sawn waveguides is presented in Fig. 4 : it shows that a very smooth surface of polymer can be achieved, here rugosity is less than 15 nm.

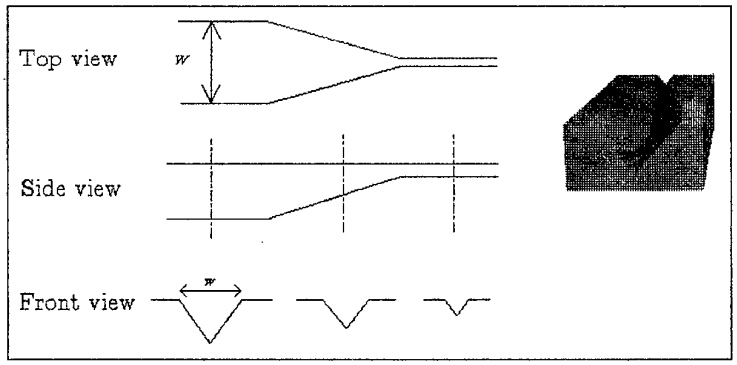


**Figure 3.** Optical Mode Transformer based on preferential etching

**Figure 4** : Photography of input facet

We have performed fibre-to-fibre measurements. First, top-diffused light has very low intensity, indicating smooth sides of waveguide. Insertion losses of a 20 to 5 $\mu$m- large transition was about 5 dB, with a contribution of about 3dB coupling losses. Such a transformer is an alternative to couple a cleaved fibre to a typical InP based optical waveguide.

## 3. Conclusion

We have proposed two different types of mode transformer to be used in monolithic or hybrid photonic integrated circuits. The first is made of three thin quaternary epilayers inserted in InP, the complete structure being grown above the classical waveguide structure. The second is made of a U-groove filled with polymer. The measurements demonstrate that these two technologies allow to improve the coupling efficiency between a typical InP/GaInAsP/InP waveguide and a monomode cleaved fibre.

# Heterostructure Solder Bumps for Optoelectronic Integration

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Abstract

This paper presents the Heterostructure Solder Bump (HSB) concept for achieving wafer-level, batch assembly of pseudo-monolithic heterogeneous integrated circuits, and describes how it is being used for optoelectronic integration. Two current technologies exploiting this concept, Epitaxy-on-Electronics (EoE) and Aligned Pillar Bonding (APB) will first be reviewed and examples of optoelectronic integrated circuits produced using EoE and APB will be described. The bulk of the presentation will then focus on the next generation HSB technology, Magnetically-Assisted Statistical Assembly (MASA), which is currently under investigation. MASA offers great flexibility and promises to be a universal heterogeneous integration technique.

Extended Summary

The challenge of integrating optoelectronic devices such as LEDs and laser diodes with complex integrated electronic circuits is one that has defied solution, beyond chip-by-chip hybrid assembly using flip-chip solder-bump technology dating from the mid-1960's, supplemented by substrate thinning and/or removal. While this approach is sufficient for prototype optoelectronic integrated circuits (OEICs) it is clearly inadequate for economic large scale OEIC manufacturing.

This talk will present pseudo-monolithic integration techniques developed at MIT suitable for wafer-scale batch processing of sophisticated OEICs. These technologies have the common feature of beginning with commercially processed integrated circuit wafers containing all of the necessary electronic circuitry. These wafers also contain recesses to accomodate optoelectronic devices. These recesses, which are typically 4 to 6 microns deep and a few tens of microns in extent, are etched into the thick dielectric overcoat covering the wafers. Using one of several techniques the recesses are then filled with III-V heterostructures for optoelectronic devices (i.e., with "heterostructure solder bumps"). After all the recesses on a wafer are filled, processing of the wafer continues to convert the heterostructures into devices and to monolithically connect them to the pre-existing electronics. The several techniques to be descibed differ primarily in the method used to fill the recesses with heterostructures; the subsequent processing is essentially identical.

The most mature of the techniques is Epitaxy-on-Electronics (EoE), in which direct epitaxy is done on chips with recesses extending all the way to the substrate. GaAs integrated circuits are used and a number of different OEIC chips have been fabricated in this way [2]. In the second technique, Aligned Pillar Bonding (APB) the heterostructures are located in the recesses by aligned metal-to-semiconductor bonding [3]. This approach has the advantage that the heterostructures can be grown on their optimal substrate under the optimum conditions, whereas with EoE the integrated circuit substrate must be used and all epitaxial processing must be done at under 475°C. The APB technique can also be used with silicon-on-sapphire circuits because the

thermal expansion coefficient of sapphire closely matches that of GaAs. It also can be used with InP-based heterostructures, and with it three-dimensional integration is possible, allowing increased packing densities.

The next stage in the evolution of these processes is magnetically-assisted statistical assembly (MASA). MASA, which is in the early stages of its development, removes all of the limitations EoE and APB place on the integrated circuit foundation. Any integrated circuit wafer can be used, and any heterostructure (or several different heterostructures) can be integrated on it because the latter are located in the recesses as individual heterostructure nanopills (or solder bumps) 5 to 6 microns thick and 30 to 50 microns in diameter (depending on the device). The process, illustrated in Figure 1, uses statistical assembly and relies upon having highly symmetrical nanopills and recesses, on providing many more nanopills than recesses, and on using magnetism to hold the nanopills in the recesses. Together these features insure that 100% of the recesses will be filled. As in all of the HSB techniques, post-assembly processing of the heterostructures insures accurate alignment of the integrated devices.

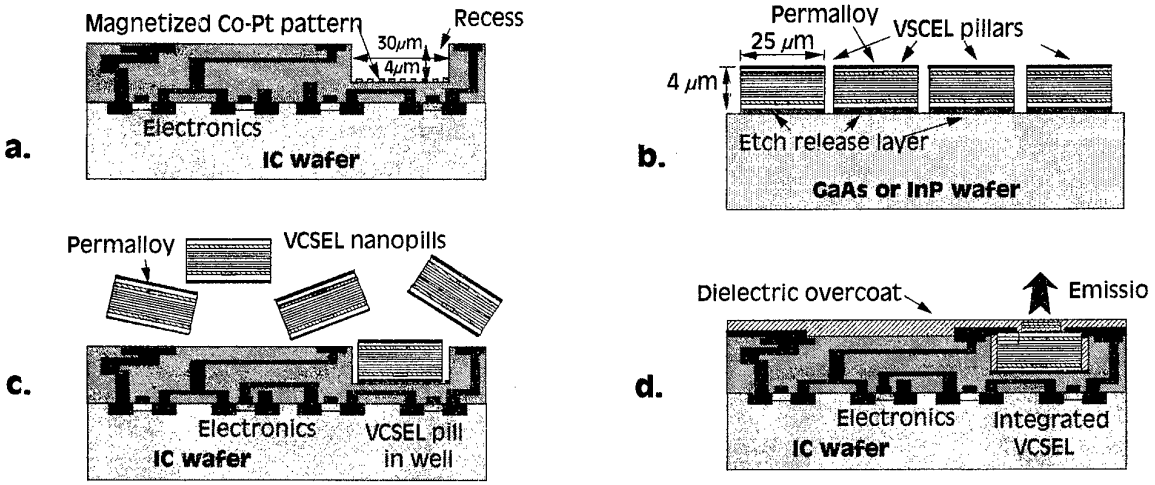


**Figure 1 -** The MASA process: (a) the processed IC wafer with the recesses prepared, and (b) the heterostructure wafer with pillars etched in a close-packed array; (c) statistical assembly of the freed nanopills in the recesses on the IC wafer; and (d) after completing device processing and integration.

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# Performance optimization of GaAs-based terahertz photomixer

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Various tasks related to the material structure and device design of GaAs-based photomixer are addressed. Properties of the mixer for application in CHAMPS, i.e. as a 490 GHz radiation source, are demonstrated. It is shown that the output power of the photomixer can be increased by optimizing the finger contact configuration as well as by improving the heat dissipation conditions.

## Introduction

Generation of terahertz radiation by photonic techniques like difference-frequency mixing in low-temperature GaAs photodetectors (LT GaAs PDs) is studied extensively [1]. However, all these efforts show that the output power needs to be increased to be useful in applications [2]. In this contribution various tasks on the preparation and performance of LT GaAs photomixer in order to increase its output power are discussed and the photomixer performance at 490 GHz is presented.

## Experimental

Two kind of LT GaAs devices were used: 50×50 $\mu m^2$ PDs to study their basic properties in the dark and under 'one-color' illumination and 5×8 $\mu m^2$ PDs coupled to the dipole antenna for 'two-colors' mixing experiments ($\lambda \cong 780$ nm). Details about the material structure and device preparation were published elsewhere [3].

## Results

Short carrier lifetime and high carrier mobility are two basic requirements on the properties of LT GaAs layer from the output power point of view. Both can be optimized by appropriate growth conditions. The layers used exhibit carrier lifetime of 150 fs (Fig. 1), which is even lower than found in LT GaAs PDs with 550 GHz bandwidth [3]. The carrier mobility was adjusted by optimizing the band and hopping conductivity ratio of the layer [4]. MSM PDs with interdigitated finger contacts were prepared using these LT GaAs layers. Responsivity measurements (Fig. 2) show that quantum efficiency of $\eta$=0.15 (no antireflection coating) can be obtained before breakdown ($V_{br} \cong 50$V). However, the $\eta$ will be lower at a mixing experiment ($P_{in}$=30 mW) because of $\sim V^2$ dependence (full dots in Fig. 2) and lower $V_{br}$. This indicates an importance of higher as possible $V_{br}$.

The photomixers (Fig. 3) are designed in the first step for 490 GHz CHAMPS (Carbon Heterodyne Array of MPIfR Systems) and perspective for GREAT systems (German Receiver for Astronomy at THz) operating at 650 GHz in SOFIA (Stratospheric observatory for infrared astronomy). From the mixing experiments (Fig. 4) it follows that the mixer bandwidth is higher than 490 GHz (1/f-dependence) and resulting conversion efficiency is comparable to previously published data [5,6]. However, the output power is still low for reasonable applications.

They are various possibilities in optimizing the photomixer performance, like by using Bragg reflectors below the LT GaAs layer to improve absorption conditions [2] or by growing thick AlAs interlayer for better thermal conductivity [6]. We concentrated at first in improving the breakdown voltage of the structures. It can be done by optimizing the finger contact geometry (Fig. 5.) Further, we developed novel structures with buried contacts which improve the electric field distribution [2] and thus the responsivity R (Fig. 6). From these follows a significant increase of the output power, as $R \sim V^2$ and $P_{out} \sim R^2$.

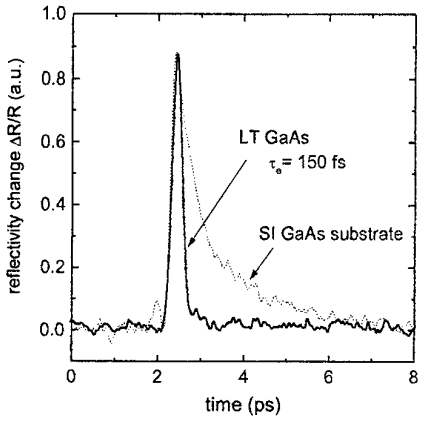


Fig. 1. Time-resolved reflectivity measurements for carrier lifetime evaluation.

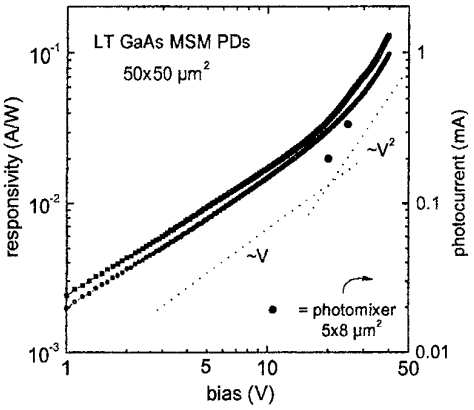


Fig. 2. Responsivity vs bias and photocurrent at 20 and 25 V at 490 GHz mixing experiment.

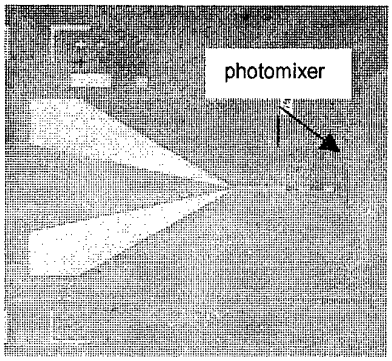


Fig. 3. Photomixer chip with 5x8 μm² detector, a dipol antenna and contact pads.

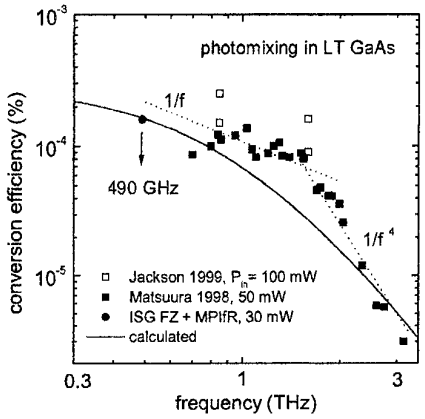


Fig. 4. Conversion efficiency vs frequency.

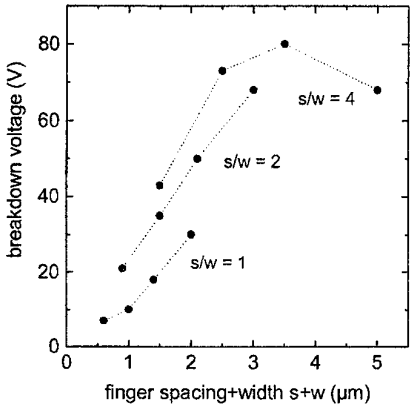


Fig. 5. Breakdown voltage for LT GaAs MSM PDs with various contact geometry.

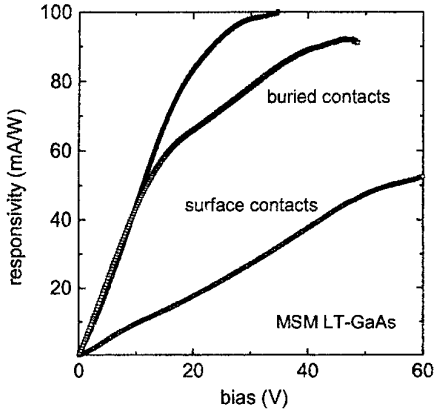


Fig. 6. Responsivity vs bias for photomixers with surface– and buried–contacts configuration.

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# Comparison of traveling-wave and lumped-element 1.55 $\mu m$ photomixers for generation of THz radiation

M. N. Feiginov and V. Krozer

*Technical University of Chemnitz, Professur für Hochfrequenztechnik, Chemnitz, Germany.*

**Abstract.** Performance of both travelling-wave and lumped-element p- i-n photomixers is compared in the THz frequency range. Our simulation results show that conversion efficiency ( $P_{THz}/P_{opt}$ ) of the lumped-element photomixer should be higher than that of the travelling-wave one up to the frequency of approximately 300GHz.

A promising technique for CW generation of the electromagnetic radiation in the THz frequency range is photomixing based on low-temperature (LT) grown GaAs or p- i-n photodiodes. Lumped-element photomixers are $RC$-time limited, that means that the generated THz power ( $P_{THz}^{lump}$ )decreases with frequency with at least 6dB/octave, when $\omega RC >> 1$. To overcome this limitation the traveling-wave (TW) photomixers were proposed and presently they are actively studied. It is generally believed that TW photomixers should outperform lumped-element ones, since they are, generally speaking, not $RC$-time limited. Nevertheless, one should meet a number of stringent requirements designing TW photomixer: the waveguide impedance should be matched to that of the antenna or output circuit, the propagation velocity of the THz wave and that of the optical wave should also be matched, attenuation of the THz wave should be made sufficiently low. Because of these limitations the lumped-element photomixers can outperform TW ones in a certain frequency range. The objective of the paper is to determine what are the frequencies where the performance of much more complicated TW photomixers is higher than that of the analogous lumped-element ones.

The THz output power of the lumped-element photomixer ( $P_{THz}^{lump}$ ) is equal to:

$$P_{THz}^{lump} = \alpha_{quant} \frac{R}{2} \left( \frac{eP_{opt}}{\hbar\omega_{opt}} \right)^2 \frac{1}{1+(\omega RC_{lump})^2}$$

where $e$ is the electron charge, $P_{opt}$ and $\hbar\omega_{opt}$ are the mean power and photon energy of the optical wave, respectively; $R$ it the impedance of emitting antenna or output circuit, $C_{lump}$ is the capacitance of the photomixer and $\alpha_{quant}$ is the quantum efficiency of the photomixer that represent an effective number of electrons generated in the contacts by one optical photon (in particular, the coefficient includes effects of the finite photocarrier transit and life times).

The similar equation for THz power generated by the TW photomixer ( $P_{THz}^{TW}$ ) is:

$$P_{THz}^{TW} = \alpha_{quant} \left( \frac{eP_{opt}}{\hbar\omega_{opt}} \right)^2 \frac{1}{2c^* C_{TW}} \alpha_{coupl}$$

here $C_{TW}$ is the capacitance of the THz waveguide per unity of length in the direction of wave propagation, $c^*$ is the effective propagation velocity of the optical wave, $\alpha_{coupl}$ is the output coupling efficiency of the THz wave due to impedance mismatch of the THz waveguide of photomixer and that of antenna or output circuit. TW waveguide is supposed to be ideal in the sense that attenuation constant of THz wave is negligibly small and the propagation velocities of the THz and optical waves are matched.

Let us compare the THz output powers of the TW photomixer and the lumped-element one. The last one is supposed to be just a short part of the TW photomixer, its length should be small as compared to wavelength of the THz wave in the waveguide. The capacitance of such lumped-element photomixer is $C_{lump} = C_{TW} l_{lump}$, where $l_{lump}$ is the length of the lumped-element photomixer. The ratio of the generated THz powers is:

$$\frac{P_{THz}^{TW}}{P_{THz}^{lump}} = \alpha_{coupl} \frac{1+(\omega R C_{lump})^2}{2c^* R C_{TW}}$$

$\alpha_{quant}$ is exactly the same for both photomixers and it is canceled in the power ratio.

The THz waveguide characteristics and the power ratio ( $P_{THz}^{TW} / P_{THz}^{lump}$ ) of the TW and corresponding lumped-element p-i-n photomixers have been calculated for a typical photomixer structure. The wave impedance of the TW structure is of the order of $10\Omega$, that corresponds to $\alpha_{coupl} \approx 1/6$, if the antanna or output circuit impedance is $50\Omega$. The length of the lumped-element photomixer is supposed to be equal to $50\mu m$. The simulation results show (see Figure 1.) that the lumped-element photomixer outperforms the TW one up to the frequency of $250GHz$. The frequency should be even higher, if the effects of the velocity mismatch and THz-wave attenuation are taken into account. If $\alpha_{coupl} \approx 1/1.2$, then $P_{THz}^{TW} / P_{THz}^{lump} > 1$ at the frequencies higher than $100GHz$. To realise the situation when $P_{THz}^{TW} < P_{THz}^{lump}$ up to $1THz$, $\alpha_{coupl}$ should be less than $0.01$.

To conclude, we have shown that the lumped-element photomixers outperform the TW ones up to comparatively high frequencies.

This work was supported by MPIfR, Bonn, Germany within ALMA Project, ESO (Agreement No.59608/MAP/00/6750/RFI).

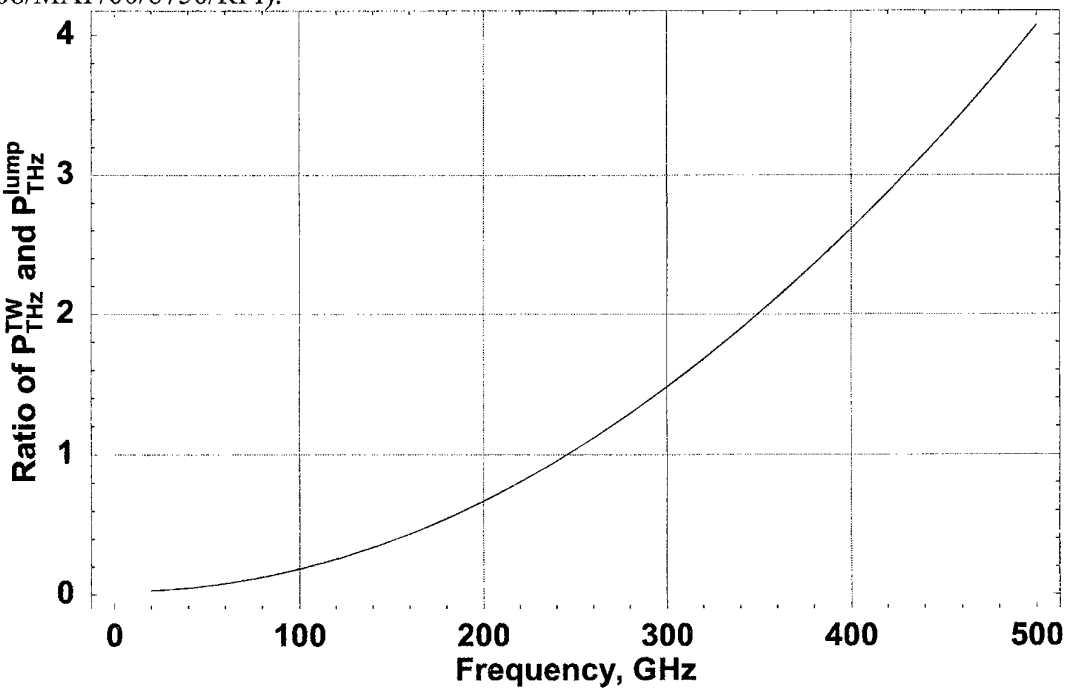


Figure 1. The ratio of the generated output THz powers of the TW and lumped-element photomixers.

# SESSION VIII
# Device and Material characterization
# Chair: Prof. Arvydas Matulionis
# Tuesday May 29, 2001

| | |
|---|---|
| **2.00 pm**<br><br>**INVITED** | **The low frequency noise in electronic devices: an engineering sight**<br>*M. Borgarino and F. Fantini*<br>Dipartimento di Scienze dell'Ingegneria and INFM, Universita' di Modena e Reggio Emilia, via Vignolese 905, 41100 Modena, Italy |
| **2.25 pm** | **Noise Behavior Of Advanced SiGe HBT**<br>*L. Bary[a], G. Cibiel[a], J. Ibarra[a], O. Llopis[a], R. Plana[a], J. Graffeuil[a], G. Niu[b], J.D. Cressler[b], Z. Jin[b], S. Zhang[b], A.J. Joseph[c] and M. Borgarino[d]*<br>(a) LAAS-CNRS and Université Paul Sabatier, 7 av. du Col. Roche, 31077 Toulouse Cedex 4, FRANCE<br>(b) Department of Electrical and Computer Engineering, Alabama Microelectronics Science and Technology Center, 2000 Brown Hall, Auburn University, Auburn, AL 36849, USA<br>(c) IBM Microelectronics, Essex Junction, VT 05401, USA<br>(d) Dipartimento di Scienze dell'Ingegneria and INFM, Universita' di Modena e Reggio Emilia, via Vignolese 905, 41100 Modena, Italy |
| **2.40 pm** | **IBIC Analysis of Gallium Arsenide Schottky Diodes**<br>*C. Manfredotti[a,b], E. Vittone[a,b], F. Fizzotti[a,b], A. LoGiudice[a,b], F. Nava[c]*<br>(a) Dip. Fisica Sperim., Università di Torino, INFN-Sez. di Torino, via P.Giuria 1, 10125 Torino (I)<br>(b) INFM- Unità di Torino Università, via P.Giuria 1, 10125 Torino (I)<br>(c) Dipartimento di Fisica, Universitá di Modena, Via Campi 213/A, 41100 Modena, Italy |
| **2.55 pm** | **Electrical and optical properties of resonant tunneling structures with interdigitated gates.**<br>*S.A.Vitusevich[a], A.E.Belyaev[b], N.Klein[a], W.Reetz[c], A.Förster[a], S.V.Danylyuk[b] and D.I.Sheka[d]*<br>(a) Inst. für Schichten und Grenzflächen, Forschungszent. Jülich, D-52425, Germany<br>(b) Institute of Semiconductor Physics, NAS of Ukraine, 03028 Kiev, Ukraine<br>(c) Institut für Photovoltaik, Forschungszentrum Jülich, D-52425, Germany<br>(d) Radiophysics Faculty, National Taras Shevchenko University of Kiev, 03127 Kiev, Ukraine |
| **3.10 pm** | **Carrier Mobility in a Forward-Biased Junction**<br>*A.R. St.Denis, D.L. Pulfrey and M. Vaidyanathan*<br>Department of Electrical and Computer Engineering University of British Columbia Vancouver, BC V6T1Z4, CANADA |
| **3.25 pm** | **Surface Acoustic Wave Investigation of the Near-Surface Layers Under Light Irradiation**<br>*D.V. Lioubtchenko[a], I.A. Markov[b], T.A. Briantseva[b], V.E. Lyubchenko[b]*<br>(a) Radio Laboratory, Helsinki University of Technology, P.O. Box 3000, FIN-02015 HUT, Finland. Tel: +358 9 451 2246, Fax: +358 9 451 2152, email: dmitri@cc.hut.fi<br>(b) Institute of Radioengineering and Electronics, Russian Academy of Sciences, 103907 Moscow, Russia. |

# The low frequency noise in electron devices: an engineering sight

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## Introduction

The term "low frequency noise" is often associated to physics. Nevertheless the low frequency noise is a powerful investigation tool for engineering. It can be useful applied by an engineer working in the technological process field or involved in the design of microwave circuits as well as operating in the reliability field.
Aim of the present work is to point out that the low frequency noise is a flexible engineering tool spanning the whole production cycle (see Figure 1). The examples, that will be addresses in the talk, are briefly itemized in the following.

## Material Growth and Technological Process

The low frequency noise is a sensitive tool to investigate the effect of the gate film composition in MOS field effect transistors [1]. The lowest noise magnitude is got by using thermal oxide while the introduction of nitrogen in the film gate increases the noise magnitude of several times. This was ascribed to the increase of interface state density [1].
The quality of the cleaning phase carried out before the emitter deposition in Si/SiGe Heterojunction Bipolar Transistor (HBT) can be efficiently addressed by looking to the noise power spectral density of the base current fluctuations [2]. The use of an HF instead of a standard cleaning technique reduces the base current noise of about two order of magnitude. Transmission Electron Microscopy microanalysis found this noise reduction correlated with an improvement in the quality of the deposited emitter film [2].
The low frequency noise can be applied also in the world of the III-V compound semiconductor HBT's [3]. GaAs-based HBT's featuring compositionally abrupt base-emitter junction exhibit a noise magnitude lower up to about 20dB with respect to HBT's with a graded base-emitter junction. A noise reduction of about 5dB was also observed as a consequence of the passivation of the HBT extrinsic base region.

## Microwave Design

The low frequency noise has to be carefully taken into account during the design of microwave oscillator, because it is up converted near the carrier reducing the oscillator spectral purity, that is increasing the phase noise [4-6].
Lorentzian components in the low frequency noise of a MOSFET degrades the phase noise of the oscillator where it is employed [5]. The use of a MOSFET without lorentzian components allowed to improve the phase noise of a Colpitts oscillator at 900MHz of about 10dBc/Hz at an offset of few kilohertz's from the carrier.
With the goal of reducing the impact of the low frequency noise on the phase noise the active device operating point can be optimised in the oscillator design [7]. In this way, a good phase noise performances of –90dBc/Hz at an offset of 100kHz from the carrier were obtained in a X-band GaAs HBT based, MMIC, fully integrated Voltage Controlled Oscillator [7].

## Reliability

The low frequency noise has been frequently suggested as a useful investigation tool in the reliability field for several active devices as GaAs-based HBT's (see for instance [8,9]), GaAs-

based High Electron Mobility Transistors (HEMT's, see for instance [10,11]), optoelectronic devices (see for instance [12,13]), Si/SiGe HBT's [14,15], MOSFET's (see for instance [16,17]), and BJT's (see for instance [17]).
Low frequency noise measurements revealed that hot holes and hot electrons life tests carried out on Si/SiGe HBT's can not be considered equivalent [14].
The comparison of low frequency noise spectra allows to distinguish between low and high reliability GaAs HBT's [8] even if, generally speaking, this procedure has to carefully applied, because the noise magnitude depends not only on the concentration but also on the position of the defects, as it is well pointed out in [17].
Even if the investigations have been frequently carried out in terms of noise power spectral density, the use of correlated quantities allows to investigate more in depth the occurring degradation mechanisms in AlGaAs/InAlGaAs HEMT's [11] and in Si/SiGe HBT's [15].
The low frequency noise found applications also in the investigation of the electromigration in the metal lines of integrated circuits (see for instance [17,18]).

**Conclusions**

The previous selected examples collected in the recent literature shows that the low frequency noise is a tool exhibiting a high degree of flexibility and interdisciplinary, offering a possible common plane to improve the exchange of information between engineers oft working in specialised sectors speaking different languages.

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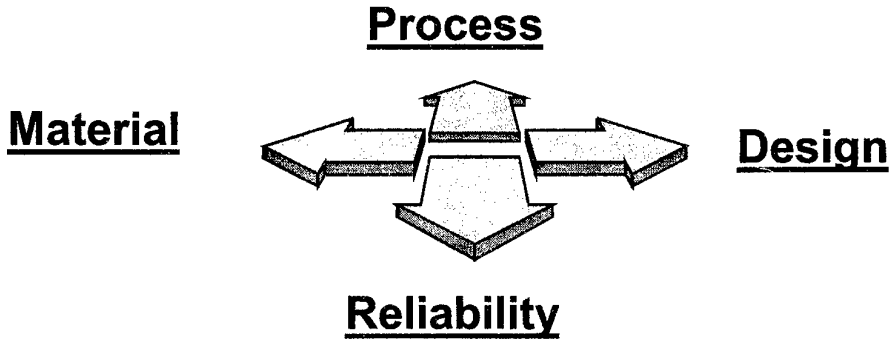


**Figure 1**: the production cycle starts from the material growth and goes through the device fabrication process, pursuing toward the design of the application and the following reliability evaluation. In each phase the low frequency noise finds applications.

# Noise Behavior Of Advanced SiGe HBT

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## I-INTRODUCTION

SiGe HBT technology has been approved for RF applications like mobile phone or Wireless local area network with frequency up to 6 GHz. Today we are seeing a fantastic explosion of what is called the "wireless society" and the associated frequency range will go to the millimeter wave range. The previous requirements in term of noise linearity, power consumption, reliability and cost are still valid and some time they are exacerbated specially concerning the noise aspects due to the spectrum saturation, the increase bit rate and the increase of the potential users. All these new changes are motivating researches in order to push SiGe technology to the millimeter wave range. In the same time, the SiGe technology CMOS compatible has to be kept in order to still have the opportunity to integrate on the same chip the analog and the digital modules. There is two possible ways to get device featuring higher frequency performance. The first one consists to shrink the device size. But it is known that usually, it turns to a degradation of the low frequency noise magnitude and then a degradation of the spectral purity of the microwave source. Furthermore shrinking the device size enhances the outdiffusion of the base dopant which is again a bad effect concerning the noise behavior of the device. The outdiffusion effect can be overcome by including some carbon as a co-doping in the base of the device. But so far, no demonstration has been done concerning the low frequency noise and the phase noise behavior of SiGeC base HBT. The second way we will discuss here deals with an increase of the Germanium rate which of course yields to an improvement of the frequency performance. Nevertheless, it is known that increasing the Ge rate increases the strain in the base layer due to the lattice mismatch between Silicon and Germanium. The devices discussed in this paper come from IBM. They feature Ge rate ranging from 0% to 18%.

## II- ELECTRICAL BEHAVIOR

We have performed an exhaustive characterization (including static, noise figure, S parameters, low frequency noise and residual phase noise). The devices exhibit emitter width of 0.5 µm and emitter length of 10 µm or 20 µm. Note that some device features two emitter fingers. We have shown that increasing the Ge rate turns to an improvement of the maximum oscillation frequency from 52 GHz to 67 GHz when the noise figure measured at 2 GHz comes from 0.66 dB to 0.2 dB. Similar results have been observed concerning the DC behavior as we get an increase of the current of the device when the Ge rate increases. The results are summarized intable 1. Fig.1 and Fig.2 show the low frequency noise measurements associated with the collector current and base current fluctuations respectively. We can observe that the Ge rate has no effect on the noise behavior occurring at the collector side which is relevant with the constant collector current value. Concerning the base current fluctations, the results indicate that the low frequency noise magnitude decreases with the Ge rate which is again relevant with the base current value. It is shown that there is no degradation associated with the Ge rate meaning that the strain management in the structure has been optimized. Residual phase noise measurements have been performed from a 3.5 GHz microwave source. Results are reported in fig.3 where we can observe that increasing the Ge rate results to an

improvement of the residual phase noise behavior which is consistent with the behavior we observed on the low frequency noise measurements. This result is very attractive as it means that it will be possible to realize microwave oscillator at higher frequency with a better phase noise performance. One very important issue deals with the location of the low frequency noise sources and residual phase noise measurements with appropriate termination are a very efficient way to clarify this point. Fig.4 presents reisudal phase noise measurements with low frequency short circuit termination. The results indicate that it results to an improvement of the noise magnitude (See table 2) confirming the physical location of noise sources at the input and at the ouput of the device. We will present a low frequency noise model that will be embedded into a microwave software to predict the phase noise of microwave oscillator.

| peak Ge in the base | None | 10% | 14% | 18% |
|---|---|---|---|---|
| β (current gain) at $V_{BE}$=0.7V | 67 | 114 | 350 | 261 |
| $BV_{CEO}$ (V) | 3.5 | 3.2 | 2.7 | 2.7 |
| peak $f_T$ (GHz) | 38 | 52 | 52 | 57 |
| peak $f_{max}$ (GHz) | 57 | 64 | 62 | 67 |
| $NF_{min}$ (dB) @ $J_C$=0.1 mA/μm$^2$ and f=2 GHz | 0.66 | 0.43 | 0.21 | 0.20 |

***Table 1:*** *Summary of electrical characteristics of the devices.*

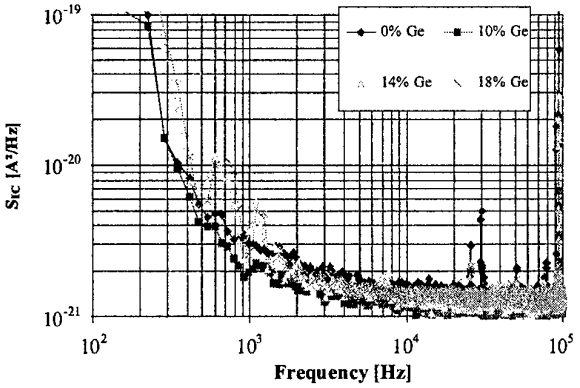


*Figure 1: Evolution of $S_{IC}$ versus different Ge content ($J_C$=1kA/cm$^2$, $V_{CE}$=1V, emitter area=10μm²)*

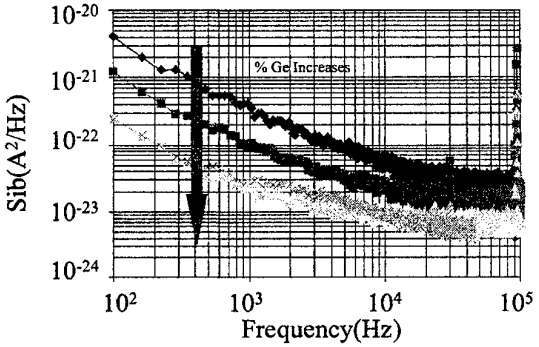


*Figure 2: Evolution of $S_{IC}$ versus different Ge content ($J_C$=1kA/cm$^2$, $V_{CE}$=1V, emitter area=10μm²)*

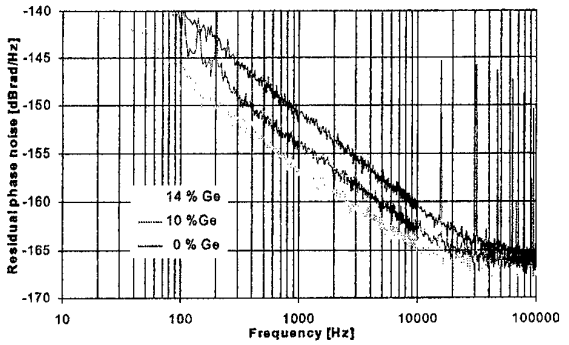


*Figure 3: Residual phase noise with three different Ge profiles, 0%, 10% and 14% ($J_C$=4kA/cm$^2$, $V_{CE}$=1V, emitter area=10μm²)*

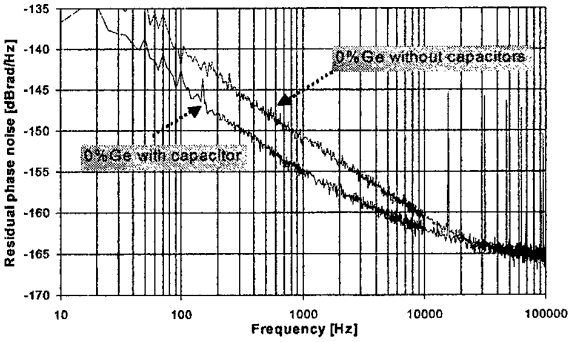


*Figure 4: Residual phase noise with and without capacitors at the input and the output of the transistor (0% Ge, $J_C$=4kA/cm$^2$, $V_{CE}$=1V, emitter area=20μm²)*

| | Residual phase noise @ 1 kHz (dBc/Hz) | Residual phase noise @ 10 kHz (dBc/Hz) |
|---|---|---|
| Without capacitors | | |
| 0 % Ge | -151 | -160.5 |
| 10% Ge | -154 | -162.7 |
| 14% Ge | -157 | -164 |
| With capacitors | | |
| 0% Ge | -155 | -162.3 |
| 10% Ge | -157.8 | -163.5 |
| 14% Ge | -159.5 | -165.4 |

*Table 2: Comparison of the residual phase noise measured with and without capacitors at the input and the output of the devices*

# IBIC ANALYSIS OF GALLIUM ARSENIDE SCHOTTKY DIODES

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Semi insulating (SI) gallium arsenide (GaAs) devices operating as a reverse biased Schottky diode offer an attractive choice as radiation detector at room temperature both in high energy physics experiments and as x-ray image sensors. However, SI GaAs devices contain a high concentration of traps, which decreases the charge collection efficiency (cce), and affects also the energy resolution of such detectors working as nuclear spectrometers in cases of a partial depletion of the detector by the external bias. A factor which greatly affects the energy resolution is given by a spatial nonuniformity of cce distribution in the electrode area.

In this paper we present a detailed investigation of the spatial uniformity of the charge collection efficiency carried out by analysing ion beam induced charge (IBIC) maps obtained by scanning a focused 2 MeV proton microbeam on a SI n-GaAs Schottky diode. The microbeam irradiated both the front (Schottky) and back (ohmic) contacts in order to evaluate the transport properties of both electrons and holes generated by ionisation. Moreover, lateral IBICC measurements were performed in order to evaluate the electric field profile.

The detectors studied in the present work were made on commercially available SI LEC undoped <100> oriented GaAs substrates with n-type resistivity $\rho \sim 10^7$ Ωcm. They were intentionally doped with C atoms in order to compensate for the presence of EL2 traps. Sample L was given a concentration of $3x10^{14}$ $cm^{-3}$, while sample A had a higher concentration ( $8x10^{14}$ $cm^{-3}$ ). The fabricated detectors were (100 ± 6) μm thick with: i) circular Schottky contacts (2 mm in diameter) realised on the front side by Ti/Pt/Au metallization and ii) uniform ohmic contacts realised on the whole back surface by e-beam deposited Au/Ge/Ni metallization. A 2 mm hole on the sample holder was made in order to allow the back contact to be irradiated.

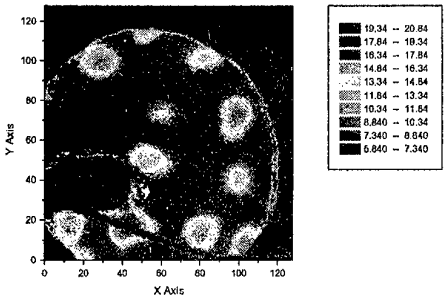
The ion beam induced charge (IBIC) measurements were performed with the proton beam intensity maintained as low as possible (less than 300 protons/s) in order to avoid saturation and pile-up of the electronic chain and space charge creation. The dimensions of the 2 MeV proton microbeam spot was about 8 $\mu m^2$ and the charge signal was recorded as a function of the beam position. The charge collection efficiency measured for protons impinging on the front electrode is primarily due to the electron drift in the detector, whereas for the back side exposure, the cce is primarily due to hole drift. The charge collection efficiency was evaluated by normalising the pulse height to the response, obtained in the same experimental conditions, of a Si surface barrier detector whose cce was assumed equal to 100%.

Detector A , front irradiated, showed a collection efficiency of about 80 %, with a saturation at about 100 V bias voltage, with an almost flat behaviour of the energy resolution ( 1 - 1.5 % ) as a function of the bias voltage in the interval 50 and 400 V. In back irradiation, cce was lower ( 80 % above 250 V ) while the energy resolution was slightly better ( below 1 % ). Energy resolution showed a strong inhomogeneous broadening, because in the homogeneous regions energy resolution was much lower than 1 %. An inhomogeneous broadening was also observed at largest bias voltages, which was apparently related with the small circular region close to the contact boundary and it was tentatively attributed to the start of an almost full, electrical field induced, collection of charge carriers generated by protons impinging externally, but very close to the electrode. As a matter of fact, due to the particular geometry adopted for the contacts, the depletion region moves also externally, since the back electrode is much larger than the frontal one.

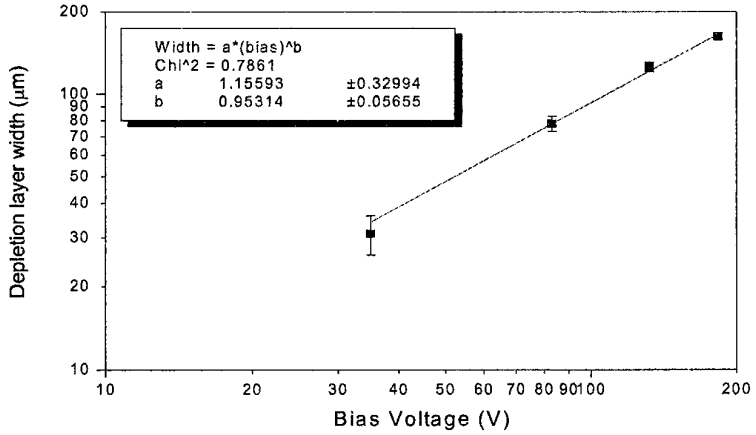
Detector L, front irradiated, displayed a collection efficiency of more than 90 %, but a worse energy resolution, not better than 2 %, with a maximum of 4 % at lower bias voltages. In fact, several regions of dimensions 200 - 300 mm were present in IBIC maps which were not connected with any possible presence ( powder, etc. ) or effect ( different thicknesses of the electrodes, etc. ) not to be attributed to the sample itself. As a proof, regions of different starting cce ( at lower bias voltages ) were followed as a function of the bias voltage itself : the ratio between the cce's varied below saturation, indicating regions with different values of (mobility)x(lifetime) $\mu\tau$ products for charge carriers. This fact could be taken as a proof that carbon helps in the homogeneisation of cce, but in conclusion lowers the cce itself.

Finally, lateral IBIC measurements were carried out on cleaved cross-sections of GaAs detectors in order to

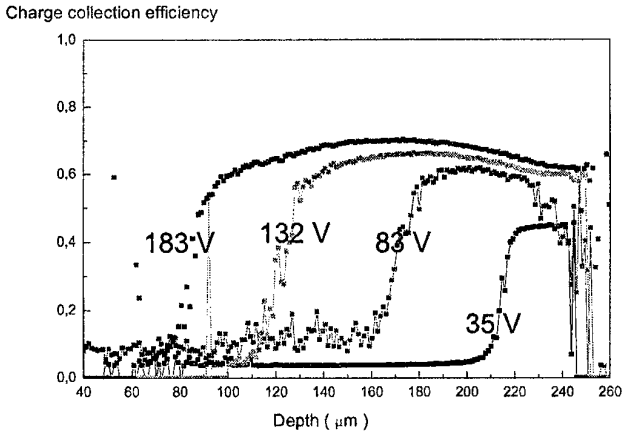
investigate the behaviour of cce as a function of depth and of the bias voltage. Profiles of cce were almost uniform in depth for cce values below 60 %, i. e. in cases in which a linear relationship is expected between cce and collection length, which is represented by the product of $\mu\tau$ and electrical field E. As a consequence, E is uniform in the depletion region and Schottky barrier is in fact a Mott barrier, with a distribution of space charge only at the border of the depletion region. Since in our case the penetration depth of protons is more than 30 μm, this is a proof of a previous result obtained by surface techniques.. The behaviour of depletion layer width vs. bias voltage was almost linear, with a power dependence with an exponent of about 0.95, in good agreement with previous results.




Frontal IBIC map of represented sample L - Bias voltage 30 V - Charge collection efficiency is by a colour scale




Behaviour of depletion layer width as a function of bias voltage



# Electrical and optical properties of resonant tunneling structures with interdigitated gates.

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P-i-n structures as well as Schottky diodes are the most frequently used photodetectors in the visible and mid-infrared range. An important advantage of such devices is the possibility of an intentional change of the depletion region width to provide the optimum quantum efficiency and time response. The main aim is to achieve a very low leakage current. One way could be the use of current blocking barriers embedded inside the depletion region. In that sense a double-barrier structure placed in an insulating layer of a p-i-n diode or in a depletion region of an Schottky diode seems to be very promising in fabrication of high performance photodetectors.

In this communication we present our recent results on electrical properties and spectral photosensitivity of double-barrier resonant-tunneling diodes (DBRTD) embedded in a depletion region of an Schottky contact at room temperature (Fig.1).

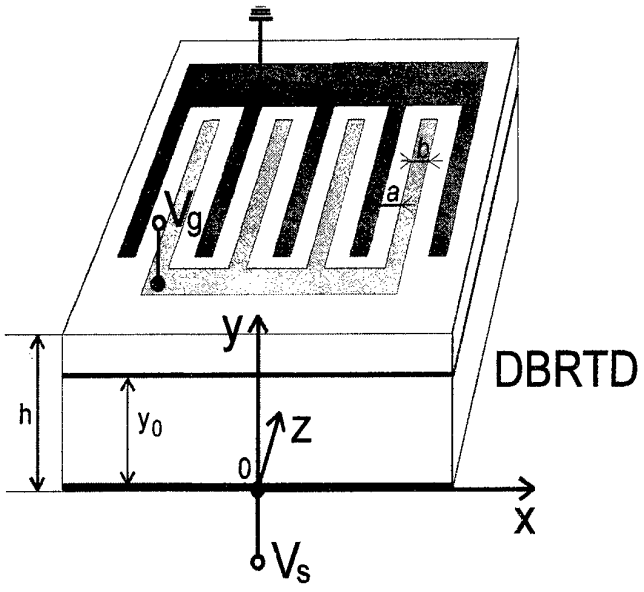


Fig.1. Double-barrier resonant tunneling structure with an interdigitated fingergates.

The structure design was as follows: the upper electrodes were placed on top of a heterostructure surface in a form of interdigitated fingergates. Each fingergate consists of 20 Ti stripes each 20 $\mu m$ long and $b$ $\mu m$ wide ($b$ = 0.5, 0.7, 1$\mu m$). The distance between the gates, $a$, is varied from 0.5 to 1 $\mu m$. The electrodes represent the Schottky contacts to the multilayer heterostructure with the barrier height $\phi_0$. The heterostructure for the measurements was grown by molecular-beam epitaxy (MBE) on a (100) $n^+$ -GaAs substrate: 200 nm $n^+$-GaAs ($n = 1x10^{18}$ $cm^3$) and 100 nm undoped GaAs spacer layers followed by a double barrier structure (2 nm AlAs barrier, 4 nm GaAs well and 2 nm AlAs barrier). An undoped GaAs layer serves as a capping layer varied from 40 to 100 nm in different devices.

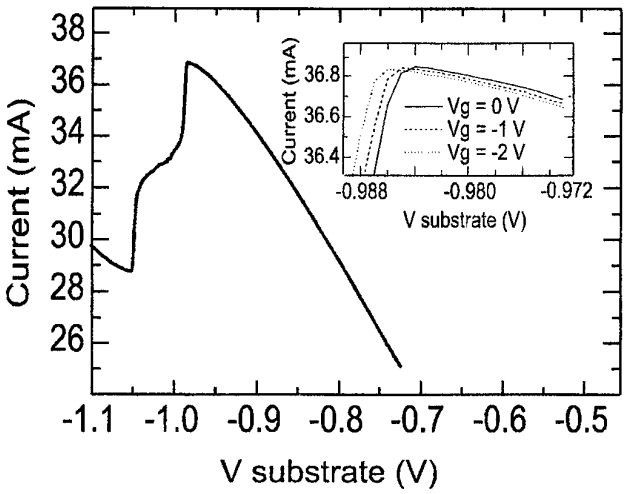


Fig.2. Current-voltage curve of the device at negatively biased substrate and $V_g = 0$. Inset: I-V curve at different $V_g$ taken in the proximity of the resonance peak.

The system of interdigitated fingergates was used to form a periodic potential profile in a multilayer heterostructure. The electrostatic problem for the spatial distribution of the potential profile was solved and experimentally examined by measurements of current-voltage characteristics of the device. Current-voltage characteristics were measured operated in transistor mode (common-drain configuration) at room temperature. Figure 2 shows the current-voltage curve of the device at a negatively biased substrate and $V_g = 0$. The resonance occurs when the Fermi level in the emitter aligns with the lowest electron level in the quantum well(QW). The position of the resonant peak voltage $V_{sr}$ is sensitive to the spatial potential distribution. In Figure 3 we present the results of the calculation of $V_{sr}$ performed for Schottky barrier height equal 0.75eV and a=b=0.53 μm. Experimental data (circles in Fig.3) are in very good agreement with the theory, which proves the validity of our model. With appropriate parameters of the heterostructure and gate design the effect could be enhanced considerably. Furthermore the formation of a potential superlattice was demonstrated. At a certain gate voltage a renormalization of the effective confinement potential transform a two-dimensional QW into a one-dimentional quantum wire array.

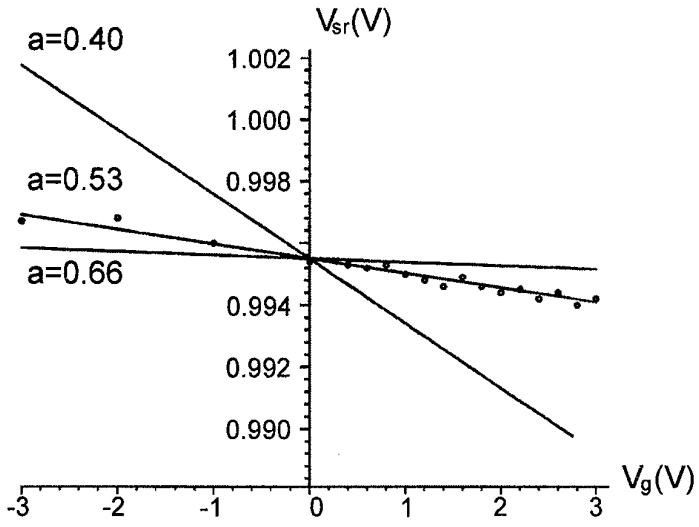


Fig.3. Dependencies of resonance voltage versus $V_g$ calculated for different spacing between gates. Circles represent experimental data.

The photoresponse characteristics of the device reveal a strong dependence on the spatial potential distribution controlled by the fingergates voltage. The device shows a very high photosensitivity. It could be interpreted with additional carrier acceleration in the built-in field of an Schottky contact.

We suppose that the Schottky diodes with the DBRTD embedded in the depletion region could find application in a new kind of electronic and optoelectronic devices.

# CARRIER MOBILITY in a FORWARD-BIASED JUNCTION

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There is a long-standing issue over the nature of the carrier mobility in a forward-biased barrier, *i.e.*, a barrier in which the net flux moves electrons up a potential energy gradient. In a reverse-biased barrier, however, it is well understood that the electron distribution is heated, and this leads to a reduction in carrier mobility. In a forward-biased barrier, however, the electron distribution is cooled, and it therefore seems reasonable that the carrier mobility should not be reduced from its equilibrium value, and may even be enhanced.

Historically, this issue may not have had much practical importance in the analysis of bipolar transistors, since their operation has been governed largely by transport through a low-field base region and a reverse-biased base-collector junction. In modern III-V bipolar transistors, however, device scaling and bandgap engineering have led to optimized devices in which transport through the forward-biased emitter-base junction may be an important factor in limiting device performance. Consequently, the issue of the nature of the carrier mobility in such regions has become one of considerable importance.

In this presentation we examine the problem by solving the Boltzmann Transport Equation (BTE) in a uniform field region, for fields which can be either retarding to electrons (as in a forward-biased junction), or accelerating to electrons (as in a reverse-biased junction). The transport is modeled via a kinetic approach, and the BTE is solved in an iterative fashion.

Results are presented for the case of isotropic, elastic scattering. They reveal that the mobility is determined by the antisymmetrical part of the electron distribution, and that this part of the distribution is the same, *regardless of the direction of the electric field.* In other words, for this type of scattering, at least, the mobility depends only on the magnitude of the electric field, and not on its direction.

In hindsight, the link between mobility and the antisymmetric distribution function appears quite natural. It has guided us to derive the following insightful equation, which appears to hold true for not only acoustic phonons, but also for scattering mechanisms particularly relevant to III-V semiconducting materials, such as polar optical phonons and ionized impurities:

$$\mu = \frac{q}{m} \frac{\int k_z f_A(\vec{k}) d\vec{k}}{\int \frac{k_z}{\tau(k)} f_A(\vec{k}) d\vec{k} - \int k_z \left[ \int f_A(\vec{k}') S(\vec{k}', \vec{k}) d\vec{k}' \right] d\vec{k}},$$

where $S$ is the transition rate, $\tau$ is the lifetime and scattering is between the states $\vec{k}'$ and $\vec{k}$.

# Surface Acoustic Wave Investigation of the Near-Surface Layers Under Light Irradiation.

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Testing of the surface and near-surface layers of $A^3B^5$ semiconductors with surface acoustic waves (SAW) propagation is effective and gives a lot of new information in addition to conventional methods of crystal morphology investigation [1]. In the previous works authors demonstrated a study of semi insulating GaAs, in which SAW was exited with interdigital transducers [2]. Unfortunately this method cannot be applied to the conductor samples because of low efficiency of the transducers.

In this work we propose a method of surface acoustic wave (SAW) diagnostics, which the investigated sample surface places at the $LiNbO_3$ plate, where SAW is exited and propagates. $LiNbO_3$ crystals are transparent for the light, so the properties of the semiconductor can be studied under white light illumination.

SAW propagation parameters (absorption and velocity as well as acceleration) give specific time-domain responses for each studied material. Besides time dependences of these data discover some different behaviors in dependence on the light and SAW intensity. Moreover it is pointing that SAW absorption and velocity changing happened due to the light exposition on the whole are caused by melting and/or mixing reaction velocities in the subsurface layers. The furrier analysis used in this case allows the spectral response of the happened reactions to be built. Such mathematical analysis may be carried out, particularly, for the second derivative magnitude time dependence. Oscillations are experimentally observed in SAW velocity time domain responses, which look like stepwise form. The spectral picture is found to be specific kind and inherent to each substance of the investigated surface acceptable as to metal so to the semiconductor and dielectric. It seems to be formed by the complex physical and chemical phenomena involved including the effect of air ionization.

The $OH^-$, $H^+$ ions besides $CO_3^{-2}$ and others as known may be formed in an air because white light illumination. Besides the molecule dipole polarization is occurred under the ultra high frequency electrical field. The SAW is accompanied with electrical field ($10^8$ Hz in our experiments). The electrical part of the SAW propagated along the piezoelectric substrate has two vectors $\vec{E}$, one of them is normal to the $LiNbO_3$ surface and influences on air molecules took place in the clearance between contacting surfaces and other is along propagating direction and influences on the surface molecules. Dipole polarization with characteristically time $\tau \approx 10^{-3}$- $10^{-9}$ s is the main kind of polarization for water consisted substance which is really the room air. As known dipole

molecules have chaotic distribution at the electrical field absence and became ordering along force line under ultra high frequency electrical field. Besides the separated micro-region may be moving relatively to each other. The SAW absorbed energy spends on the molecule excitations so in the air micro-layer took place near at the $LiNbO_3$ surface or immediately in the dielectric surface. It needs to wait for the temperature ionic polarization at the boundary with the $LiNbO_3$ surface ($\tau \approx 10^{-7}$-$10^{-13}$ s) due to the SAW absorbed energy. All of these cause the molecular interaction increasing at the boundary with $LiNbO_3$. The interaction reactions between an air and dielectric molecules result in a new compound formation, for instance LiOH, LiH, $Li_2O_3$, etc. It is achieved with rather large local energy extracting resulted in doped ion and electron arising so in the air layer near the dielectric surface.

The electrical polarization connected with free charge carriers moving to the system boundaries ($\tau_{el} \approx 10^{-4}$-$10^{2}$ s) is observed. It leads to the chemical interaction increasing also and resulted in a new compound forming (such as Me-OH or Me-O etc.) so at the $LiNbO_3$ as at the investigation sample surfaces. It is known that when two plates became concerned and one of them is heated in more degree it appears pushing off forces normally to their boundaries. At this surface faced to the $LiNbO_3$ is under the superior pressure then the back one.

Thus the plastic deformation will arise in the investigated plate followed by particle motion (they may be electrons, ions, Ga and As atoms, etc.). As a sequence of surface properties both elastic (viscosity coefficient) and electrical (charge state so as dielectric permittivity) states are changed in accordance to extent of probability for particles to be arrived to the plate surface. It leads to high frequency electro-magnetic radiation emanated from the surface of the sample putted over $LiNbO_3$. The cause of such emanation is the structure polarization of molecules free or low connected with crystal lattice. The correlation between irradiation frequency and velocity of molecules orientation relaxation ($10^{9}$-$10^{13}$ $s^{-1}$) occurs. Thus acoustic wave in the $LiNbO_3$ near-surface layer realizes under influencing of high frequency field reflected from the plate putted over. It is accompanied with direct and indirect excitation of the $LiNbO_3$ sublayer molecules resulted in its viscosity and SAW propagation characteristic changing. Here we have the arrangement looked like spectrum analyzer where charge particles source is the $LiNbO_3$ surface and the investigation sample surface is a target and ionization air is conductivity media above that $LiNbO_3$ surface with SAW propagation themselves being the perturbation detector.

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# SESSION IX
# Advanced Devices and materials
# Chair: Lester F. Eastman
# Tuesday May 29, 2001

| | |
|---|---|
| **4.00 pm**<br><br>**INVITED** | **Premature Saturation in AlGaN/GaN HFET's.**<br>*R.J. Trew*<br>EECS Department, Case Western Reserve University, Cleveland, OH. |
| **4.25 pm** | **Surface and nearsurface transformations in A3B5 semiconductors under typical technology enforcements**<br>*D.V.Lioubchenko, T.A.Briantseva, V.E.Lyubchenko*<br>Inst. of Radioengineering and Electronics, Russian Academy of Sciences, Moscow |
| **4.40 pm** | **New Concept of Antireflective Films With Silicon Oxynitrid Graded Refractive Index**<br>*L. Zighed*[(a)], *M. Remram*[(b)], *A. Abuarafah*[(b)]<br>(a) Département d'Electronique, Faculté des sciences de l'ingénieur Université Mentouri, Constantine, 25000<br>(b) College of technology Makkah, Kingdom Saudi-Arabia. |
| **4.55 pm** | **Equivalent Circuit and High-Frequency Performance of the Resonant-Tunneling diodes**<br>*M. N. Feiginov*<br>Tech. University of Chemnitz, Reichenheiner Str. 70, Chemnitz 09107, Germany |
| **5.10 pm** | **Optimisation Criteria for a Frequency Tripler with Anti-Serial Schottky Diodes**<br>*M. Krach, J. Freyer, and M. Claassen*<br>Walter Schottky Institut, Technische Universität München, Am Coulombwall, D-85748 Garching, Germany |
| **5.25 pm** | **Hexagonal Binary Decision Diagram Quantum Circuits on III-V Nanowire Networks - a Novel Approach toward Quantum LSIs-**<br>*H. Hasegawa and S. Kasai*<br>Research Center for Integrated Quantum Electronics and Graduate School of Electronics and Information Engineering, Hokkaido University, N-13, W-8, Kita-ku, Sapporo 060-8628, Japan |
| **5.40 pm** | **Surface-Related Kink Effects in AlGaAs/GaAs Power HFET's**<br>*E. Tediosi*[(a)], *G. Verzellesi*[(a)], *C. Canali*[(a)], *G. Sozzi*[(b)], *R. Menozzi*[(b)], *C. Lanzieri*[(c)]<br>(a) Dipartimento di Scienze dell'Ingegneria and INFM, Universita' di Modena e Reggio Emilia, via Vignolese 905, 41100 Modena, Italy<br>(b) Dipart. di Ingegneria dell'Informazione, Universita' di Parma, 43100 Parma, Italy<br>(c) Alenia Marconi Systems, via Tiburtina, km 12, 00131 Roma, Italy |

# *Premature Saturation in AlGaN/GaN HFET's*

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Field-Effect Transistors based upon the AlGaN/GaN heterostructure are predicted to be capable of producing RF output power on the order of 10-12 W/mm of gate periphery. This is almost an order of magnitude greater than possible from GaAs-based devices. Spot experimental results indicate performance in agreement with the theoretical predictions, and approximately 10 W/mm has been obtained in C-band and X-band. Power-added efficiency, with good gain, also approaches the theoretical expectations, at least through C-band. However, the RF performance of these devices often demonstrate premature saturation and the gain experiences compression at relatively low RF drive. It is observed that the drain current decreases with RF input drive, which is not in agreement with the normal operation of these devices. Highly non-linear performance results, which limits or precludes the application of these devices as power amplifiers in many communications and radar applications.

As shown in Fig. 1 there are several locations within the HFET where nonlinear charge behavior could produce premature saturation.

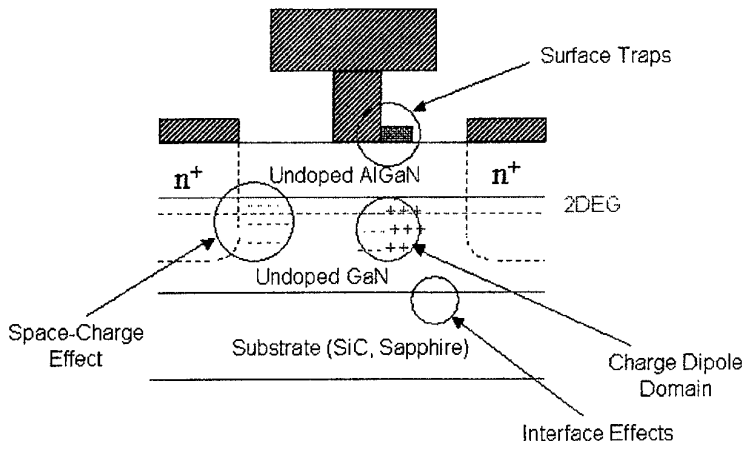


Fig. 1 HFET Sources of Nonlinear Performance

Current slump and premature saturation can be caused by a high density of surface charging states that deplete the conducting channel, thereby producing a reduction in current as the states become increasingly charged. Although surface state charging significantly affects HFET performance, these effects alone cannot explain the experimental data. Current slump and premature saturation can also occur due to space-charge suppression of the electric field in the source region. Space-charge effects occur due to the high current density at which these devices are operated (e.g., $J_{ds}$~$10^6$ A/cm), and the lack of background impurity doping that would resist space-charge effects. In the absence of surface state effects, space-charge suppression in the

source region would still produce current slump and premature saturation of the RF gain. This effect is consistent with experimental data.

It can be shown that the electric field at the source contact can be written as

$$E_0 = \frac{J(0) - q\mu_n \left(\frac{kT}{q}\right) \left.\frac{d\delta n(x)}{dx}\right|_0}{q\mu_n (n_0 + \delta n(0))}$$

where $E_0$ is the electric field, $\delta n(x)$ is the excess injected charge and $J(0)$ is the dc channel current at the source contact. The suppression of the electric field and the corresponding reduction in channel current for an AlGaN/GaN HFET is shown in Fig. 2.

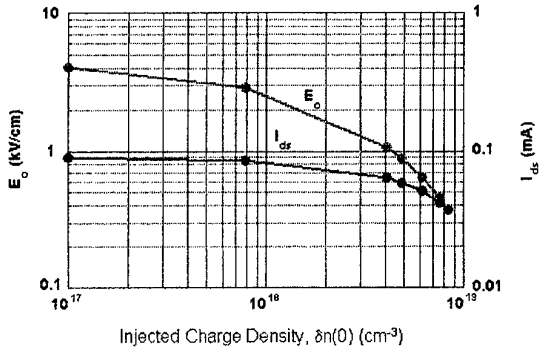


Fig. 2 Electric Field and Channel Current Suppression as a Function of Injected Charge Density for an AlGaN/GaN HFET

The reduction in channel current causes a reduction in RF output power, power-added efficiency, and gain, as shown in Fig. 3.

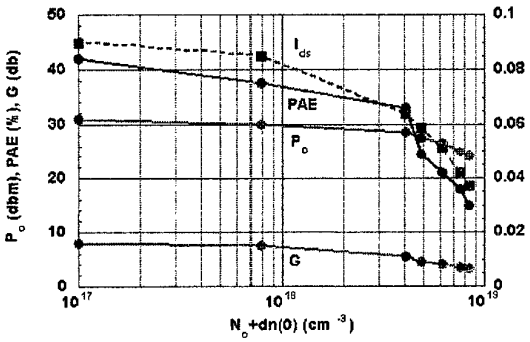


Fig. 3 RF Performance as a Function of Injected Charge for an AlGaN/GaN HFET Showing Premature Saturation

It is demonstrated that source region space-charge suppression of the electric field occurs under high-injection conditions and that this effect can cause premature saturation. Realization of linear high power amplifiers fabricated from these devices will require that the HFET be designed so that this effect is minimized.

# Surface and Near-Surface Transformations in $A^3B^5$ Semiconductors Under Typical Technology Enforcements

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The fabrication of semiconductor devices requires processes such as thermal treatment, lithography, contact deposition etc., which affect the near-surface structure and composition of the semiconductor materials. The process-induced changes can in turn affect device performance. It has been noted [1] that all structure and composition changes to the surface are accompanied by thermomechanical strains leading to point defect motion, dislocation generation etc. In the case of crystalline semiconductors, investigations of surface composition should allow the effects of such parameters as crystal tensile strain and the dynamics of the mechanical stresses in the subsurface layers to be investigated.

Lattice transformations in the near-surface layers of GaAs, InP, GaN were studied as been induced with nonthermal enforcements of the light, microwave or electron beam irradiation, mechanical compression and current flow during such actions as optical or electron beam lithography, wire bonding, vacuum deposition of thin films, which are widely used in the semiconductor device technologies. The discussed effects were indicated by chemical analysis, Auger spectroscopy, conductivity measurements and surface acoustic wave diagnostics and analyzed as a result of the plastic deformations and chemical reactions.

The observations presented in this study indicate an overall decrease in "free" Ga and As presence at the surface or otherwise crystalline GaAs after processing by ultrasonic thermocompression, current flow, electron beam irradiation, mm-wave irradiation or laser irradiation and annealing, compared with that presented prior to irradiation [2,3]. In general the "free" Ga and/or As increases gradually only after a rapid initial decrease as the process time or temperature is increased. It is well-known that "free" Ga and As atoms can be generated on the surface of crystalline GaAs by chemical reactions, such as oxidation [4], during surface treatments or during epitaxial growth due to the excess flux of one of the components in the growth chamber [1], or during thermal processing as Ga and As interstitials are generated in the bulk and diffuse to the surface, such as during laser annealing or laser assistant growth of Al film on the semiconductor surface which results in Al-Ga-N compound formation at the GaAs surface. As well as these simple thermal processes, more

complex changes can occur with dissolution of surface oxide layers or interactions e.g. with thin metal films covering the semiconductor surface. Thermal processing can also cause recovery and recrystallization, and can lead to an improvement in the crystalline quality of the near-surface region.

Free Ga and As can also be generated by surface mechanical stresses; for instance the mechanical deformation of GaAs crystals can result in diffusion of interstitial atoms towards tensile strained regions, with vacancies moving towards compressive strained regions. The force experienced by the interstitial atoms and vacancies is proportional to the pressure gradient, and the distribution of point defects will re-adjust at unloading. Stress relaxation takes place during mechanical loading, as well as when the sample deformation is held constant, and during sample heating. The relaxation processes are driven by internal stresses, generated during the preliminary deformation. In diffusion-controlled processes, the point defects may start and finish not just on the external sample surface, but also at grain boundaries, stacking-faults and dislocations.

Diffusion creep can also take place as a consequence of a variety of irradiation processes as well as thermal activation, with the point defects created by the irradiation adding to the equilibrium point-defect concentration at the irradiation temperature, promoting the rearrangement of the point defects into configurations nearer to equilibrium. For instance, vacancies will move to regions under tensile strain, and interstitial atoms to compressed regions during heating.

The irradiation procedures described above can clearly produce composition changes on the surface and near-surface layers of semiconductor devices that could result in device degradation. The experimental data shows that such changes take place by diffusion mechanisms associated with plastic deformation prior to creeping, even at the relatively low irradiation energy, which was used in this work.

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# NEW CONCEPT OF ANTIREFLECTIVE FILMS WITH SILICON OXYNITRID GRADED REFRACTIVE INDEX .

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**Abstract:** the objective of our study was to develop a new concept of antireflective films based on the use of a layer in which the refractive index vary continuously with thickness. The silicon oxynitride properties had made it better candidate for obtaining a graded refractive index for a silicon solar cells. In the absence of a general method permitting a direct calculation of the variation function of the index, which lead to the desirable optical response, we have use the optical theory of stratify medium, which permit to determine the parameters of the optimum graded antireflection coating.

**Introduction :**

The disadvantages established, in the case of use of classical antireflection coatings which had a constant index, have lead to the research of a new type of coating: a graded refractive index antireflection coating, that's mean, an inhomogeneous layer in which the index change continuously in accordance with thickness. Potentially, this system should permit to get zero reflection in a large range of wavelength and for different angle of incidence 1,2]

So, we have fixed the following objectives: show that the graded index layers minimise the reflection under the conditions of oblique incidence on the one hand, and the research of the parameters of the optimal layer on the other hand.

**Results :**

To carry the graded index our choice is bring on silicon oxynitride, because of their properties which are intermediate between those of silica and silicon nitride.

In our study, the variations of the volume fraction of $SiO_2$ in accordance with thickness e: $f_{SiO2}(e)$ are used to describe the variations of the refractive index in the layers.

Experimentally, we can realised layers in which the volume fraction of silica vary between 0.25 and 0.95.

In calculations, we have considered that the coatings studied are composed of 100 sublayers, this permit to minimise the step of the index leap . This coatings have, linear, parabolic or third polynomial degree profiles. It can be increasing or decreasing. The variation low of the volume fractions in the different profiles are shown in table 1.

**Table 1:** Variation lows of the volume fraction of silica in graded index layers

| profile | $f_{SiO2}(x)$ |
|---|---|
| linear | $-0.0071x + 0.95$ |
| parabolic | $0.0000714\ x^2 - 0.0141414\ x + 0.95$ |
| polynomial | $-0.0000007x^3 + 0.000214\ x^2 - 0.021212\ x + 0.95$ |

Where x is the number of the sub layer, it vary between 1 – 100.

First, we have optimise the thickness. The optimal layer is the one which minimise reflection in the spectral region of maximum energy. We have find that it's of 100 nm in all cases (see figure 1, case of

increasing linear gradient). Next, we have proceed to the research of the optimal coating under oblique incidence conditions. In this stage, to valid our work, we have compare the reflection factors obtained by the use of graded index layers with those obtained when the antireflective coating is a double layer of $SiO_2$ /$TiO_2$ centred on 600 nm.

So, we have obtained the curves shown in the figures 2, 3 and 4 that present factors of reflections of the different coatings under normal incidence, 45° and 80°, respectively.

**Conclusion :**

From the different results, we can say that the graded index layers minimise the reflection under oblique incidence, and that the optimal layer is the one which have a third polynomial degree increasing profile, of 100 nm thickness, in which the index vary between 1.4832 and 1.8714 at 600 nm.

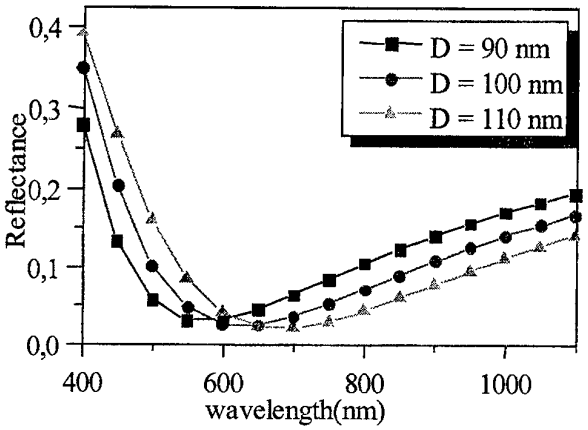


Fig.1 : Optimisation of the thickness of an increasing linear graded index coating.

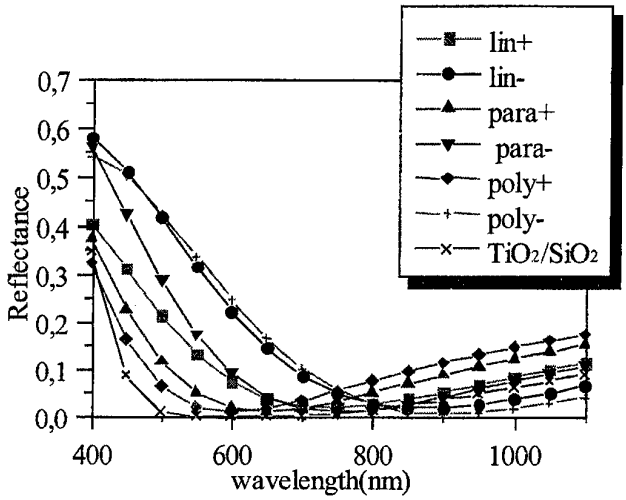


Fig.2 : Reflectance of the different graded index coatings of 100 nm thick under normal incidence.

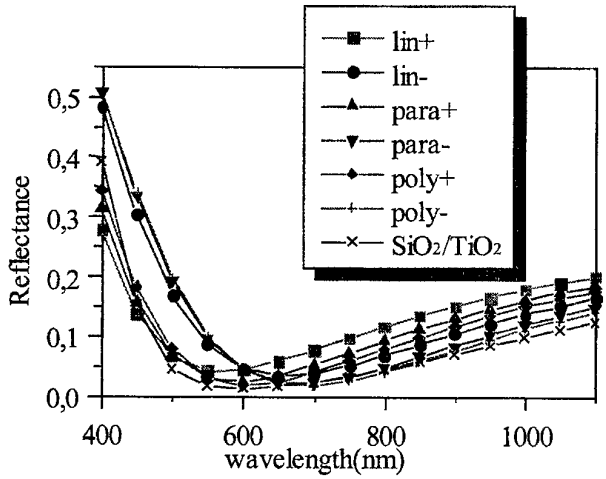


Fig.3 : Reflectance of the different graded index coatings of 100 nm thick under oblique incidence (θ= 45°).

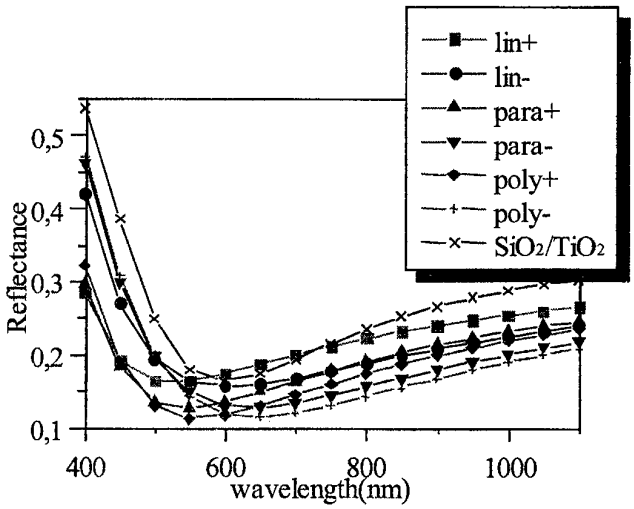


Fig.4 : Reflectance of the different graded index coatings of 100 nm thick under oblique incidence (θ= 80°).

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# Equivalent circuit and high-frequency performance of the resonant-tunneling diodes

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**Abstract.** We have shown that, first, the response time ( $\tau_{resp}$ ) of the resonant-tunneling diodes (RTDs) can be much smaller as well as much larger than the quasibound-state lifetime in the quantum well ( $\tau_{dwell}$ ). Second, the real part of the RTD conductance can be negative and large at frequencies higher than the reciprocal $\tau_{dwell}$ in the RTDs with heavily doped collector. A simple analytical expression for the impedance of RTD has been derived, it is in fairly good agreement with experimental data. An equivalent circuit is proposed.

## Introduction

2D electrons accumulate in the quantum well (QW) of the resonant-tunneling (RT) diodes (RTD) based on the double-barrier heterostructures. It has been shown recently that the Coulomb interaction of the 2D electrons with that in emitter and collector can lead to the I-V curve of Z-type in the static case. Thus far no consideration has been given to the effect of the Coulomb interaction on the response time ( $\tau_{resp}$ ) of the RTD. So far it was believed that $\tau_{resp}$ can not be less than the electron dwell times in the QW due to the tunneling to emitter ( $\tau_e$ ) and collector ( $\tau_c$ ). In the present work we show that it is not true and that $\tau_{resp}$ can be much smaller than $\tau_e$ and $\tau_c$. The Coulomb interaction should lead to the same effect in other RT structures, e.g., the quantum cascade laser, also it should be essential for the domain speed in the superlattices.

The problem of the equivalent circuit of the RTD is closely related to that of the response time. Many equivalent circuits have been proposed in the literature. Among them the simplest RC-circuit, RLC-circuit, two RC circuits connected in series are in most common use. Nevertheless, there are no a simple and yet comprehensive way to describe the impedance of the RTD. Problem is solved in the present work. The problem was dealt with in a number of papers, but the results are so cumbersome that it seems to be possible to use them just for numerical calculations.

## Results

In the present work it has been shown that:

- The response time of RTD is smaller and much smaller than the electron dwell time in the quantum well in the positive differential conductance region. In the high-quality structures with 2D $\rightarrow$2D tunneling $\tau_{resp}$ can be by the orders of magnitude less than $\tau_{dwell}$, here $1/\tau_{dwell} \equiv 1/\tau_e + 1/\tau_c$.
- The response time of RTD is principally large in the negative differential conductance (NDC) region, i.e. $\tau_{resp} > \tau_{dwell}$ and $\tau_{resp} \rightarrow \infty$ when NDC $\rightarrow -\infty$.

A simple analytical expression has been derived that relates $\tau_{resp}$ to the static differential conductance.

A quite general and simple analytical equation for the RTD conductance has been derived and also an equivalent circuit has been proposed (see Fig. 1), it fairly well describes the published experimental

data (see Fig. 2). It was shown that in the low-frequency and high-frequency limits the RTD conductance can be approximated by the RC-circuits. The low-frequency limit describes the experimentally observed features in the low-frequency capacitance. It was shown that the high-frequency conductance essentially depends on the variation of the tunnel transparency of the collector barrier with bias and that can lead to the positive value of differential conductance at high frequencies. To make the high-frequency conductance negative and large in the NDC region the collector should be heavily doped and it should not contain spacer layers. That gives possibility to use RTDs as an active element in the high-frequency generators, with the frequencies can be higher than reciprocal $\tau_{dwell}$. The value of the high-frequency conductance in this case is substantiated by the RTD geometry and $\tau_{dwell}$, it does not depend on the static differential conductance.

The work was supported by Programs FTNS (99-1124) and PAS (3.1.99); INTAS (97-11475) and RFBR (99-02-17592)

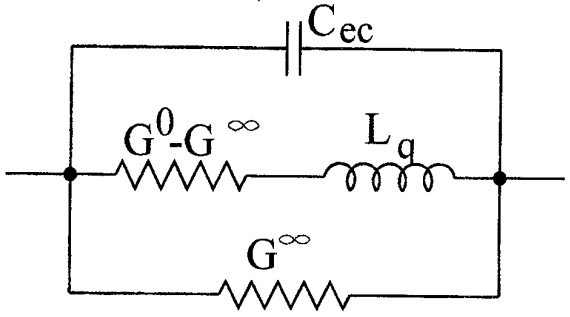


Figure 1. The equivalent circuit of RTD, here $L_q \equiv \tau_{resp}/(G^0 - G^\infty)$ is an inductance, $G^0$ is the static differential conductance, $G^\infty$ is a high frequency conductance.

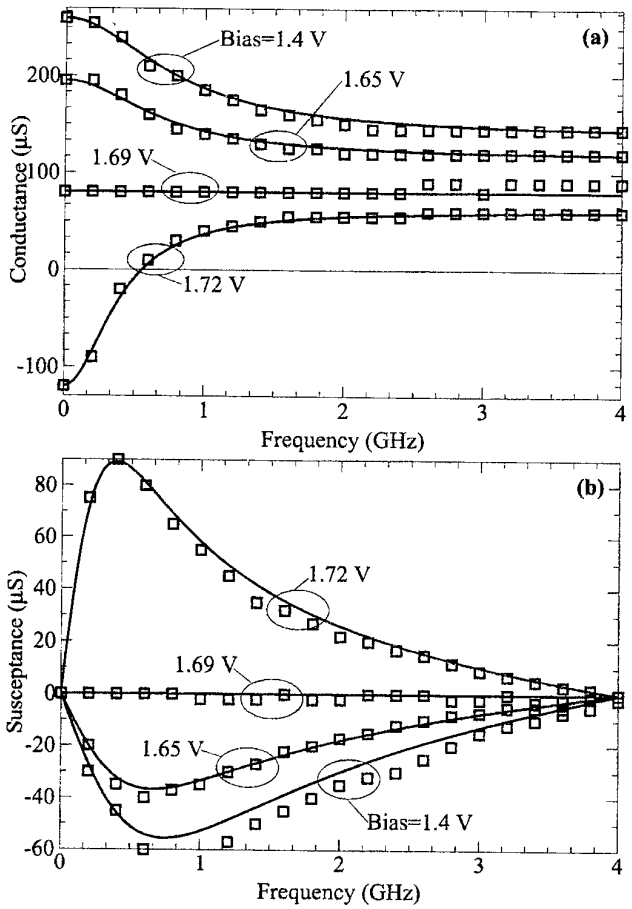


Figure 2. Comparison of the experimental data (from J.P.Mattia, et al., J. Appl. Phys. **84**, (1998) 1140) and simulation with the help of the equivalent circuit in Fig. 1.

# Optimisation Criteria for a Frequency Tripler with Anti-Serial Schottky Diodes

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*This paper describes a new type of frequency-multiplier for mm-waves [1] which combines the advantages of a varactor with symmetrical capacitance-voltage characteristic and the relatively low leakage current of Schottky diodes. The varactor structure consists of two inhomogeneously doped Schottky diodes in anti-serial connection which are quasi-monolithically integrated into a microstrip circuit on quartz. A theoretical description of the Schottky diode tripler, resulting design and optimisation criteria, as well as first experimental results are presented.*

The symmetric varactor is realized by an anti-series connection of two Schottky diodes with common Schottky contact. Since Schottky barriers sustain higher electric fields as compared to hetero-barriers used in SBVs (single-barrier varactors) [2], higher power capability and thus smaller device diameters are possible. This allows higher varactor impedance and thus less detoriation due to circuit losses.

The dynamic CV-characteristic of two anti-series diodes can be calculated from the static CV-behaviour of a single device. The latter is computed by solving Poisson's equation self-consistently. The steplike doping profile of the devices according to Fig. 1 results in an elastance-charge characteristic S(Q) with two different slopes. Due to opposite self-biasing, $S_1(Q)$ and $S_2(Q)$ of the individual devices are shifted by a charge displacement $\Delta Q$, the size of which corresponds to the amplitude of the applied signal. In Fig. 2, the shifted functions of the anti-serial diodes ($S_1(Q+\Delta Q)$, $S_2(Q-\Delta Q)$) under operating conditions are shown for a given charge modulation Q(t). The total elastance $S_{tot}$ of the two diodes is equal to the sum of the elastances of the single devices. For a high varactor efficiency, $S_{tot}$ should feature a large elastance change $\Delta S$ (see Fig. 2) demanding a V-shaped total elastance with a high gradient. However, the steepness is limited by the maximum drift velocity of the electrons in the non depleted zone since the charge modulation is determined by the drift velocity. This leads to the following optimisation criteria for the single devices:

(i) The S(Q)-characteristic has to be designed such that the kink of the elastance curve is reached at the self-bias charge $\Delta Q$ which corresponds approximately to the amplitude of Q(t),
(ii) for lower charge, the elastance should change as little as possible which can be achieved with high doping in the first zone or a doping spike, and
(iii) the slope of the elastance curve should be very steep beyond the bias charge demanding low doping in the second zone limited only by the condition that the maximum current through the device must be carried by conduction with reasonable mobility.

Taking these conditions into consideration, $\Delta S$ is not significantly higher than that of typical SBVs, however, as compared to these devices the doping concentration of the active region of the proposed anti-serial Schottky varactor can be about twice. Thus also the maximum current can be twice leading to four times higher power capability per area. Additionally, the unavoidable series resistance which lowers the cut-off frequency and efficiency of the varactor can be reduced since in the case of anti-serial Schottky diodes, large area contacts at the $n^+$-side can be used. Theoretical estimations show that an efficiency of more than 20% should be achievable.

First experimental results are realised with two anti-serial Schottky diodes according to the structure given in Fig. 1 on quartz substrate. Tripler performance was tested in a split full

height waveguide mount [2,3] (see Fig. 3) at a fundamental frequency of 70 GHz. The experimental results of this structure design show an rf-output power of 2 mW at 210 GHz with a flange to flange conversion efficiency of over 3 %. Though to this date these values are lower as compared to SBVs, significantly higher efficiency and output power are expected for a tripler with optimised anti-serial Schottky diodes, e.g. with delta-doped structures.


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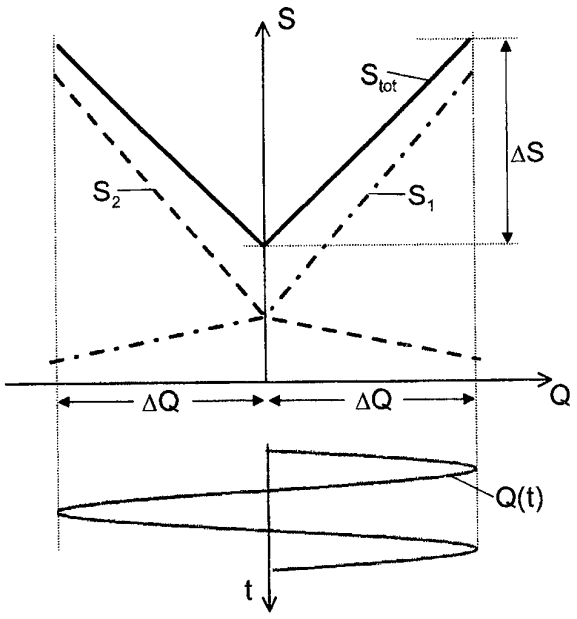


*Fig. 2: Schematic elastance-charge functions for the anti-serial Schottky diodes under charge modulation condition*

| Schottky contact | |
|---|---|
| $Al_{0.55}Ga_{0.45}As$ | d=10nm |
| $N_D = 4\times10^{18}$ | d=20nm |
| $N_D = 2\times10^{17}$ | d=200nm |
| contact layer | |
| quartz substrate | |

*Fig. 1: Schematic layer sequence of the Schottky diodes*

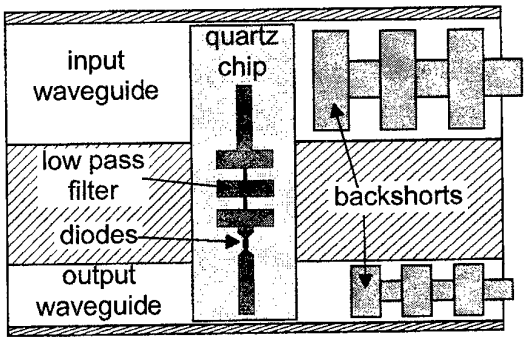


*Fig. 3: Schematical view of the waveguide mount and quartz chip*

# Hexagonal Binary Decision Diagram Quantum Circuits on III-V Nanowire Networks - a Novel Approach toward Quantum LSIs -

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A novel hexagonal binary decision diagram (BDD) quantum circuit approach for large scale integration of quantum devices is presented, and its feasibility is discussed

## Introduction

Research on quantum devices such as quantum wire transistors (QWRTrs), electron-wave transistors, single electron transistors (SETs) etc has been intensively carried out over 20-25 years. However, no realistic approach seems to exist, at present, for construction of quantum (Q-) LSIs. The major reason is the difficulty to use such "weak and environment-sensitive" devices in the conventional Boolean logic gate architecture with AND/OR gates etc which requires very "robust and uniform" devices such as Si CMOS Trs. In fact, we demonstrated recently the world first III-V quantum logic inverter with a transfer gain of 1.3 using a single electron switch[1]. However, the gain was not large enough, the drivability was small, and input-output voltage matching was difficult.

The purpose of this paper is to propose a novel approach for III-V Q-LSIs and to report on the results of our experimental investigation concerning its feasibility. In our approach, GaAs and InGaAs hexagonal nanowire networks are systematically controlled by nano-scale Schottky gates in order to implement circuits based on the binary-decision-diagram (BDD) logic architecture.

## Hexagonal Quantum Circuit Approach

Quantum BDD circuits[2] consist of arrays of BDD node devices and can realize any logic function. As shown in **Fig.1(a)**, each BDD node device sends a single or few electrons coming into the entry branch into either 0- or 1-branch, depending on gate input. In contrast to the logic gate architecture, no direct output-to-input connection is necessary, thereby requiring no large voltage gain, no precise input-output voltage matching, no large fan-in and fan-out numbers and no large current drivability. It is a good architecture for quantum devices operating near the quantum limit of delay-power product. For hardware implementation, we pay attention to the basic three-fold branch symmetry of the node device, and propose to use III-V hexagonal nanowire networks controlled by our Schottky wrap gate structure (WPG)[3] shown in **Fig.1(b)**. The present Q-LSI structure is obviously applicable, in future, to molecular nanowire networks.

## BDD Node Devices

Recently, we have already demonstrated correct path switching and realization of simple BDD logic functions, using a 3-WPG GaAs single electron Y-switch as the BDD node device[2], shown in **Fig.2(a)**. In this paper, we use new BDD node devices having a 1-WPG QWRTr or a 2-WPG SET on each of the exit branches which works complementarily, as shown in **Fig.2(b)** and **(c)**. For GaAs devices, several-100 nm-wide nanowires were made by EB lithography and wet etching. For InGaAs devices, several-10-nm-wide nanowires embedded in InAlAs barriers were

grown on patterned InP substrates by selective MBE. Each branch of the fabricated node devices exhibited clear conductance quantization and oscillation. With these, clear path switching was obtained.

## Device Integration

A GaAs hexagonal integrated two-bit quantum adder without nanowire crossover was designed and fabricated, as shown in **Fig.3(a)** and **(b)**. It showed a correct operation from 1.5 K up to at least 120 K by bias adjustments. This is because, with temperature increase, the circuits show gradual transitions from the real quantum regime with a minimum delay-power product to a few electron quantum regime, and finally to the many electron classical regime. Thus, wire size reduction should lead to room temperature operation in the quantum regime. To realize this, we have succeeded in growing submicron-pitch sub-10nm-wide InGaAs hexagonal nanowire networks by selective MBE, as shown in **Fig.4**. Future prospects using such hexagonal nanowire networks will be discussed.

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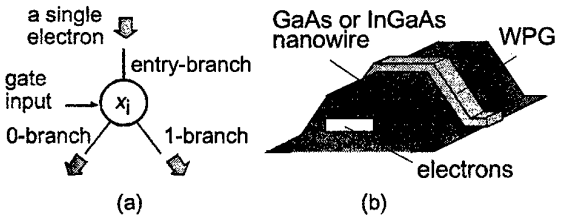


**Fig.1** (a) BDD node device (b) wrap gate structure.

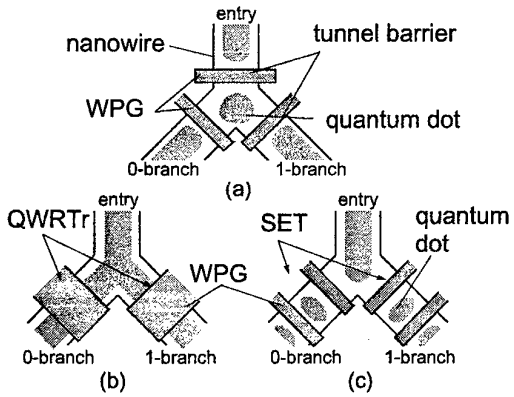


**Fig.2** Various BDD node devices. (a) single electron Y switch type, (b) quantum wire branch switch type and (c) single electron branch switch type.

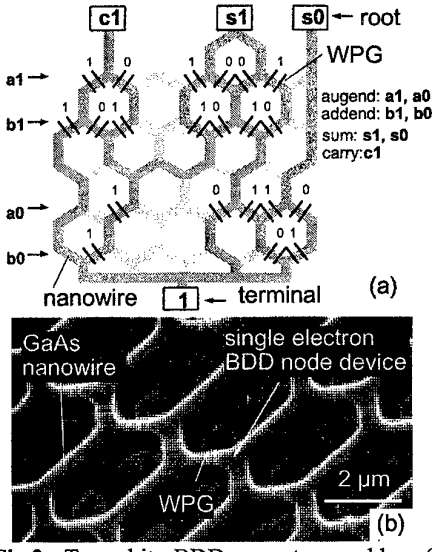


**Fig.3** Two bit BDD quantum adder (a) hexagonal layout and (b) fabricated adder.

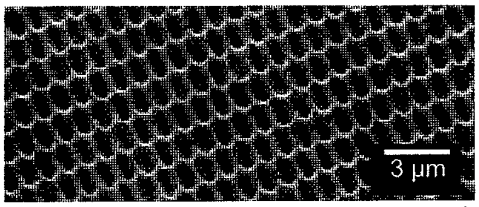


**Fig.4** A hexagonal InGaAs nanowire network by selective MBE.

# Surface-Related Kink Effect in AlGaAs/GaAs Power HFETs

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R. Menozzi (2), C. Lanzieri (3)

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An anomalous increase in the drain current at relatively-low drain-source voltages is often observed in the output characteristics of III-V compound semiconductor FETs. This phenomenon, which is usually referred to as the kink effect results in output-conductance increase, transconductance compression, and dispersion between DC and RF characteristics. Although a lot of effort and several papers have been dedicated to the kink, the physical origin of this effect is still an issue of contention [1-3]. In this paper, the kink effect is investigated in as-fabricated and hot-carrier stressed AlGaAs/GaAs power HFETs both through measurements and two-dimensional device simulations.

The cross section of the HFETs is sketched in Fig. 1, showing the following bottom-up structure: GaAs SI substrate; AlGaAs/GaAs multilayer buffer; 75 nm thick n-GaAs channel, Si-doped at $4x10^{17}cm^{-3}$; $Al_{0.25}Ga_{0.75}As$ barrier layer, Si-doped at $2x10^{17}cm^{-3}$, 30 nm thick under the gate; $n^+$-GaAs cap for low-resistance ohmic contacts. Gate width and length are 200 μm and 0.25 μm, respectively. Additional details can be found in [4].

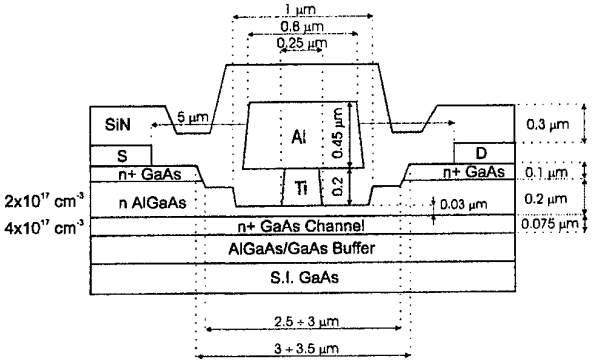


**Fig 1.** Schematic cross section of the power HFET.

Devices underwent room temperature DC accelerated stress experiments under several different bias conditions. The main degradation modes observed were a reduction of the drain saturation current ($I_{DSS}$) and of the transconductance. Both effects turned out to be strongly correlated with an increase in the drain access resistance (measured by an end-resistance method). These observations indicate a well known mechanism of degradation of the semiconductor/passivation interface over the gate-drain access region, which gets negatively charged due to electron trapping by surface states generated during the stress. In addition to that, enhancement of the kink was observed in increasingly stressed devices. Figure 2 shows typical experimental output characteristics before and after stress, demonstrating both $I_{DSS}$ reduction and kink enhancement. An exhaustive description of accelerated-stress results can be found in [4-6].

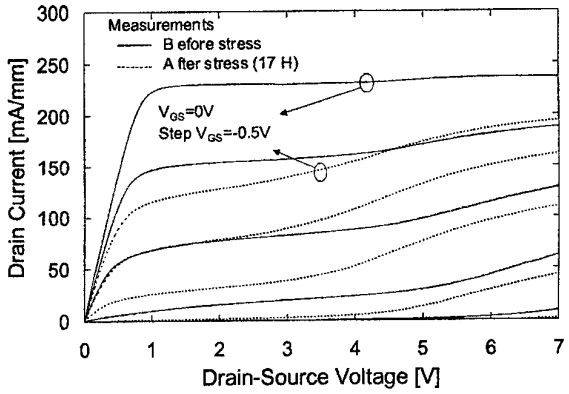


**Fig 2.** Experimental output characteristics before and after stress.

Two-dimensional numerical device simulations were performed with the program DESSIS [7], allowing both drift-diffusion and hydrodynamic transport models to be adopted. To account for surface damage, acceptor-like traps were placed at the ungated gate-source and gate-drain surfaces. Relying on current-mode DLTS measurements performed on stressed devices [5], surface traps were energetically located at 0.36 eV above the top of the valence band ($E_V$), and the capture cross sections were set to $2x10^{-17}$ $cm^{-2}$.

Figure 3 shows hydrodynamic simulations of the HFET output characteristics in the following two cases: (a) with the trap density set to $N_{TS}=N_{TD}=1x10^{12}$ $cm^{-2}$ at both gate-source ($N_{TS}$) and gate-drain ($N_{TD}$) surfaces; (b) with $N_{TS}=1x10^{12}$ $cm^{-2}$ and $N_{TD}=1x10^{14}$ $cm^{-2}$. In the former case, simulations describe the pre-stress conditions, the relatively-low trap-density value adopted at both sides of

the gate recess being representative of process-induced damage. In the latter, stress-induced surface damage is accounted for by raising $N_{TD}$ with respect to $N_{TS}$. In both cases, impact ionization is not activated in the simulator. As can be seen in Fig. 3, these simulations predict the $I_{DSS}$ reduction but are unable to reproduce the kink.

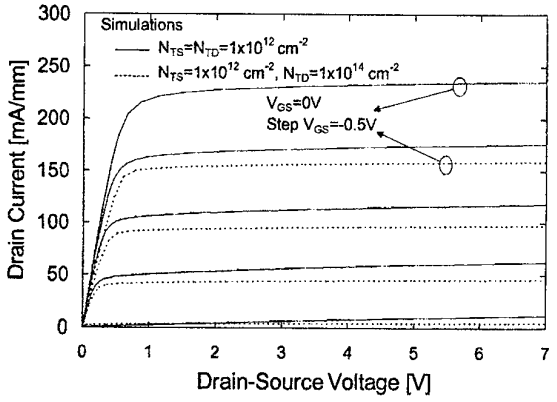


**Fig 3**. Simulated output characteristics with surface traps but without impact ionization.

Figure 4 shows output characteristics obtained from hydrodynamic simulations for different $N_{TD}$ values (and fixed $N_{TS}$) and with the impact-ionization model activated. In this case, simulated output characteristics feature a kink. The latter becomes smaller and smaller as $N_{TD}$ is reduced, finally disappearing when $N_{TD}$ is made lower than $2x10^{12}$ cm$^{-2}$. This result is consistent with measurements (see Fig. 2) demonstrating kink enhancement in increasingly stressed devices.

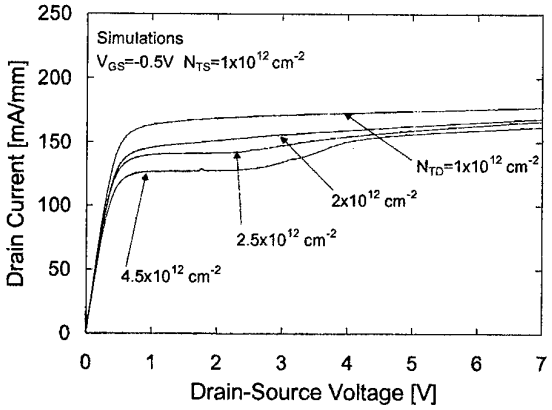


**Fig 4**. Simulated output characteristics with both surface traps and impact ionization.

The physical mechanism originating the kink is elucidated by Fig. 5, showing the electron density along a vertical cut under the gate and the source and drain ungated regions at two $V_{DS}$ values (preceding and following the kink). As can be seen, at $V_{DS}$ =2 V (< $V_{kink}$), the conductive channel is narrower in the drain access region than in the source one, due to the higher negative surface charge. By increasing $V_{DS}$ beyond $V_{kink}$, the conductive-channel width is only marginally affected under the gate and in the source access region, whereas it widens in the drain access region as the gate-drain surface charge gets partially compensated by impact-ionization-induced holes, resulting in drain-current increase and kink.

In conclusion, we have shown that, differently from what generally accepted for GaAs- and InP-based HEMTs, where the kink is attributed to accumulation of impact-ionization-induced holes in the source access region [1,2], the kink arises in AlGaAs/GaAs HFETs from the combined effect of impact ionization and traps located at the gate-drain recess surface. Kink enhancement after hot-electron stress is a consequence of trap-density increase at this surface.

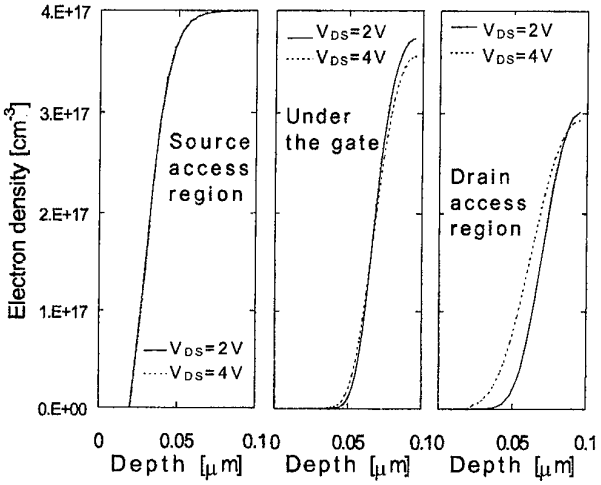


**Fig 5**. Simulated electron density as a function of depth under the gate and in the source and drain access region at $V_{DS}$ values preceding and following the kink voltage ($V_{kink}$≈ 3V), $V_{GS}$= -0.5V, $N_{TS}$= 1 ×$10^{12}$ cm$^{-2}$, $N_{TD}$= 4.5 ×$10^{12}$ cm$^{-2}$

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# SESSION X
# GaN-based devices
# Chair: Prof. Joachim Wuerfl
# Wednesday May 30, 2001

| | |
|---|---|
| **8.30 am**<br><br>**INVITED** | **GaN on Silicon for High Power and High Frequency Electronics**<br>*Dr Eddie Piner*<br>Nitronex Corporation, 628 Hutton Street, Suite 103 Raleigh, NC 27606. |
| **8.55 am** | **High Frequency Noise Studies in AlGaN/GaN MODFETs**<br>*S. S.H. Hsu[(a)], D. Pavlidis[(a)] J. S. Moon[(b)], M. Micovic[(b)], C. Nguyen[(b)], and D. GriderJeong[(b)]*<br>(a) Department of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor, MI 48109-2122, USA<br>(b) HRL Laboratories, 3011 Malibu Cyn. Rd., Malibu, CA 90265 |
| **9.10 am** | **Optimization of AlGaN/GaN HEMT structures using the RoundHEMT technology**<br>*M. Marso[(a)], P. Javorka[(a)], A. Alam[(b)], M. Wolter[(a)], H. Hardtdegen[(a)], A. Fox[(a)], M. Heuken[(a)], P. Kordoš[(a)], and H. Lüth[(a)]*<br>(a) Institute of Thin Films and Interfaces, Research Centre Juelich, D-52425 Juelich, Germany<br>(b) AIXTRON AG, Kackertstr. 15-17, D-52072 Aachen, Germany |
| **9.25 am** | **Characterization of Temperature Dependence of AlGaN/GaN HEMTs**<br>*T. Mizutani, M. Akita and S. Kishimoto*<br>Department of Quantum Engineering, Nagoya University, Furo-cho, Chikusa-ku, Nagoya, 464-8603, Japan |
| **9.40 am** | **Influence of Barrier Thickness on the High Power Performance of AlGaN/GaN HEMTs**<br>*V.Tilak, B.Green, J.Smart, J.R.Shealy, L.F.Eastman*<br>Electrical and Computer Engineering, Nanofabrication facility, Cornell University, Ithaca NY, 14853-5401 |
| **9.55 am** | **An investigation into the charge distribution and pinch off behavior of AlGaN/GaN double heterostructure DH-FETs under Schottky and ohmic contacts.**<br>*M.Zervos, A.Kostopoulos, G.Constantinidis, M.Kayambaki, S.Mikroulis and A.Georgakilas.*<br>Foundation of Research and Technology Hellas (FORTH), Institute of Electronic Structure and Laser (IESL), Microelectronics Research Group (MRG), Vassilika Vouton, Heraklion 711 10,Crete,Greece. |

# GaN on Silicon for High Power and High Frequency Electronics

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Lee McCarthy, and Ricardo Borges
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## Introduction
*

The family of materials known as wide-bandgap semiconductors offers a powerful set of electronic properties. Among these, gallium nitride has emerged as a top candidate for high frequency and high power devices. The excitement surrounding GaN stems from its unique material and electronic properties summarized in Table 1. While silicon and GaAs come up short on simultaneously handling high frequencies and high power, GaN is perfectly suited to achieve optimum performance for these applications. GaN devices can support internal electric fields much higher than can silicon or GaAs. This property is useful for handling high power and for obtaining higher efficiencies through the use of higher supply voltages. Other equally key properties of GaN include its high electron saturation velocity and its high electron mobility, both of which contribute to its strength at high frequencies. Furthermore, there have been breakthroughs recently in producing high quality GaN on convenient substrates, such as silicon.

Despite its beneficial properties, GaN high frequency high power devices have yet to appear on the market. The most important reason is that until recently, GaN material development for high power and high frequency electronics has concentrated on sapphire and SiC as the conventional substrates of choice, both of which have significant disadvantages for potential commercial applications. GaN on sapphire offers a relatively medium cost substrate choice, compared to silicon and SiC, and has a longer history of GaN material development. However, sapphire is a poor thermal conductor that results in thermally limited devices and can only be obtained in up to four-inch diameters in limited quantities. SiC substrates, on the other hand, are excellent thermal conductors, offer a closer lattice match to GaN, and can achieve as good material quality compared to sapphire. The limiting factors for manufacturing GaN devices on SiC are the excessive substrate cost associated with semi-insulating SiC, the limitation of wafer diameter size availability, and a high density of substrate related defects reducing device yields.

From prior art investigations; GaN epitaxially grown on silicon is generally of lower quality than GaN grown on sapphire or SiC. This has been due to the large lattice and thermal mismatch between the Si substrate and the GaN film. Other issues include the nitridization of silicon, Si autodoping into the GaN at high growth temperatures, and the subsequent cracking associated with the aforementioned lattice and thermal mismatch. However, the fundamental advantages of silicon over SiC and sapphire have driven a recently renewed interest in this material for, primarily, optoelectronic but also transistor applications. These advantages include very low cost substrates, large area wafers, and the highest quality substrate from the point of view of defects and surface quality.

* SIGANTIC™ is a trademark of Nitronex Corporation

**Table 1. Electronic Material Properties**

| *Property* | *Si* | *GaAs* | *SiC* | *GaN* |
|---|---|---|---|---|
| **Energy Gap (eV)** | 1.11 | 1.43 | 3.2 | 3.4 |
| **Breakdown Field (V/cm)** | $6 \times 10^5$ | $6.5 \times 10^5$ | $3.5 \times 10^6$ | $5 \times 10^6$ |
| **Electron Saturation Velocity (cm/sec)** | $1 \times 10^7$ | $2 \times 10^7$ | $2 \times 10^7$ | $2.5 \times 10^7$ |
| **Electron Mobility ($cm^2$/V-sec)** | 1500 | 6000 | 800 | 1600* |

* AlGaN/GaN heterostructure mobility.

## GaN on Silicon Material Breakthroughs

GaN epitaxial growth directly on silicon is hindered due to the large lattice and thermal mismatch between GaN and silicon. A number of different techniques have been employed to counteract these problems.[1-6] All techniques rely on a buffer layer that is situated between the silicon substrate and GaN film. It is interesting to note that a similarly functioning layer is also necessary to be able to obtain high quality GaN on sapphire or SiC. Silicon, however, has turned out to be much more of a challenge.

The primary problem associated with epitaxial GaN on silicon is the propensity of the GaN film to crack due to thermal and lattice mismatch between GaN and silicon. In the past, the typical critical thickness for the onset of cracking was ~0.4μm. This thickness of GaN could be used to grow device structures, however, GaN on Si is very much like GaN on sapphire and SiC in the sense that the dislocation defect density is influenced by the GaN film thickness. For very thin films, the dislocation density is very high. As the GaN film thickness increases, the dislocations have a tendency to form loops and annihilate one another thereby reducing the overall defect density at the surface. For 0.4μm GaN on Si, the dislocation density is very high and device performance is hindered accordingly.

At Nitronex Corporation we have developed a breakthrough transition layer that alleviates the problem with cracking and allows for the growth of much thicker GaN epitaxial films. The effect of this transition layer is illustrated in Figure 1 where GaN epitaxial films grown with and without the transition layer is shown. Clearly, the crack density has been substantially reduced for a film with a thickness on the order of 2μm. This growth technique, known as the SIGANTIC process, involves an engineered process that accommodates the differences in lattice and thermal coefficient of expansion mismatch between epitaxial nitride layers and the silicon substrate. Thick (>2μm), crack-free epilayers can be obtained with very smooth interfaces by this technique.[7]

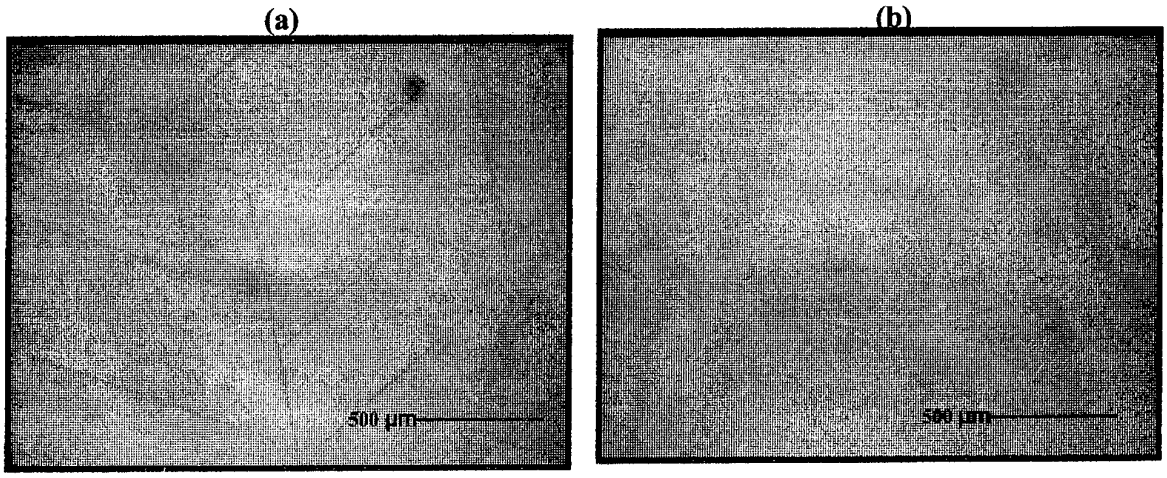


**Figure 1. GaN on Si without (a) and with (b) the SIGANTIC growth technique.**

### AlGaN/GaN on Silicon HEMT Structures

AlGaN/GaN high electron mobility transistor structures have been grown on silicon using the SIGANTIC growth process. High electron mobilities are necessary for high frequency performance to minimize internal device delays. High electron velocities can be obtained by using modulation doped heterostructures. Among the wide-bandgap semiconductors, the III-nitride material system is the only one to offer a heterostructure system as shown in Table 2. This means that GaN-based devices are uniquely able to exploit the power handling capabilities of wide-bandgap semiconductors as well as the high frequency potential of modulation doped structures.

**Table 2. Key Material Issues for High Frequency, High Power Transistors**

| *Property* | *Si* | *GaAs* | *SiC* | *GaN* |
|---|---|---|---|---|
| **Suitability for High Power** | Medium | Low | High | High |
| **Suitability for High Frequencies** | Low | High | Medium | High |
| **HEMT Structures** | No* | Yes | No | Yes |
| **Low Cost Substrates** | Yes | No | No | Yes |

*May change with ongoing Si/SiGe heterosystem research.

The HEMT structures that have been grown include both undoped and Si-doped AlGaN/GaN heterostructures. The AlGaN layer is pseudomorphically strained and gives rise to a piezoelectric polarization induced charge at the AlGaN/GaN heterointerface. This, coupled with the spontaneous polarization of the heterojunction, gives rise to very high two-dimensional electron gas (2DEG) carrier densities in tandem with high electron mobilities, as shown in Table 1. The simplest structure is the undoped AlGaN/GaN structure. It is also common to incorporate a Si-doped AlGaN layer into the heterostructure to increase the charge density of the 2DEG. In that case, an undoped AlGaN spacer layer is inserted to minimize the effect of ionization impurity scatter in the 2DEG.

Through the utilization of the SIGANTIC growth technique to obtain thick, high quality GaN buffer layers and the employment of the HEMT structure to the GaN on silicon process, we have obtained electron mobilities greater than 1600cm$^2$/V-sec at a sheet electron charge greater than 1.0x10$^{13}$cm$^{-2}$. These numbers represent the highest ever reported for GaN on silicon and are comparable to the current state-of-the-art transistor structures grown on sapphire and SiC. From these epiwafers, AlGaN/GaN HEMT devices have been fabricated and tested and will be discussed in more detail.

## Conclusions

GaN on silicon offers a low cost, highly manufacturable platform for high power, high frequency devices. The fundamental electronic aspects of the III-nitride material system makes it ideal for use in these types of applications while the low cost of silicon makes it the best choice for the manufacturing of such devices. A new growth technique has been developed that allows thick GaN films to be deposited on silicon without the common side effect of cracking. Coupling this growth process with AlGaN/GaN HEMT structures has resulted in state-of-the-art performance for GaN on Si. These breakthroughs in GaN growth on silicon are expected to bring GaN electronic devices to market in the near future.

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# High Frequency Noise Studies in AlGaN/GaN MODFETs

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Impressive microwave and high-power performance have been demonstrated from AlGaN/GaN MODFETs[1]. DC, microwave small-signal and large-signal characteristics of these devices have been reported by various researchers. However, only little work addressed the noise characteristics of GaN-based FETs[2]. In this study, AlGaN/GaN MODFETs grown using RF-assisted MBE on sapphire substrate were characterized and device noise performance was evaluated.

The measured devices in this study had a gate length of 0.25 μm, a gate finger width of 200 μm. The device structures consist starting from the substrate of an undoped GaN buffer, an NID $Al_{0.22}Ga_{0.78}N$ spacer, n-$Al_{0.22}Ga_{0.78}N$ donor layer and an NID $Al_{0.28}Ga_{0.78}N$ cap layer. The fabricated devices exhibited excellent DC and microwave characteristics. A maximum drain current density of ~ 1.35 A/mm and a peak transconductance of ~ 320 mS/mm were obtained. Fig. 1 shows the device's maximum oscillation frequency ($f_{max}$) and cut-off frequency ($f_T$) under various bias conditions. As can be seen, these devices show a maximum $f_{max}$ ~ 81 GHz ($V_{GS}$=-3.4 V, $V_{DS}$=15 V), and $f_T$ ~ 57 GHz ($V_{GS}$= -2.6 V, $V_{DS}$= 15 V).

The minimum noise figure ($F_{min}$) was characterized at 10GHz under $V_{DS}$= 10 V as a function of drain current and the results are shown in Fig. 2. A minimum noise figure of 1.9 dB with 16.2 dB associated gain was obtained at a quiescent point of $I_{ds}$= 30 mA for the device used in this study. Noise figures of 0.7dB were measured for 0.15μm long gate devices using the same technology. The variation of $F_{min}$ was found to be relatively small in the measured current range. In addition, $F_{min}$ was also found to be relatively independent of drain bias voltages within the measured range of 5-15 V. Results indicate that AlGaN/GaN MODFETs can maintain a small value of $F_{min}$ over a wide bias range, which is a good feature for relaxed circuit design. $F_{min}$ as a function of frequency was also evaluated and shown in Fig. 3. Within the measured frequency range, $F_{min}$ varied from 1.47 to 2.92 dB. The associated gain ($G_a$) values were found to decrease monotonically from 16.5 to 12.0dB. As a result of this change, the input-referred noise was increased. Fig.4 shows the extracted noise resistance ($R_n$) vs. drain current; $R_n$ is a measure of the sensibility of $F_{min}$ to the changes of the input admittance with respect to its optimum value. Results show these devices exhibit a value of ~ 20-30 Ω, which is compatible with values reported for InP-based Hemts [3].

The noise characteristics of the AlGaN/GaN Hemts were analyzed in an attempt to provide an explanation for their good noise figure values. Special attention was paid to the impact of the reduced gate leakage current compared with the traditional III-Vs due to the wide bandgap materials used in GaN-based devices. A simple analytical equation can be used to explain the noise characteristics of FET-type devices [4]:

$$F_{\min} = 1 + 2\frac{f}{f_c}\sqrt{\alpha\beta(1-C^2)}$$

where $f$ is the operating frequency, $f_c$ is the intrinsic cut-off frequency and α, β and $C$ are fitting coefficients corresponding to drain noise current, gate noise current and gate-drain noise correlation. One can see the gate noise current also contributes to the value of $F_{min}$. The gate noise current is dominated by the gate leakage current (GLC). GLC effects introduces not only a parasitic conductance at the device input, but also adds shot noise. It has been shown that the noise performance of MESFETs and MODFETs are strongly dependent on the gate leakage current value [5]. The AlGaN/GaN devices measured in this study exhibit a gate current density ($J_G$) ~ $2\times10^4$ A/m$^2$ to $8\times10^4$ A/m$^2$ as $V_{DS}$ varies from 0-15 V (Fig. 4), which is small compared to the theoretically expected value for the onset of gate-leakage current having an effect on $F_{min}$ for the pseudomorphic MODFETs [5]. In addition, values of the shot noise current contributed from gate current were also calculated using the $2\cdot q\cdot I_G$ expression. As can be seen in Fig. 4, the noise currents are extremely small over a wide bias range. This is a possible reason for the observed relatively bias independent $F_{min}$ characteristics.

In summary, the high-frequency noise of AlGaN/GaN MODFETs was characterized under various bias conditions and frequencies. $F_{min}$ was found to be relatively constant over a wide range of drain bias currents and voltages. The reduced gate leakage current due to the use of GaN wide bandgap materials is contributes in the excellent noise performance of GaN-based MODFETs.

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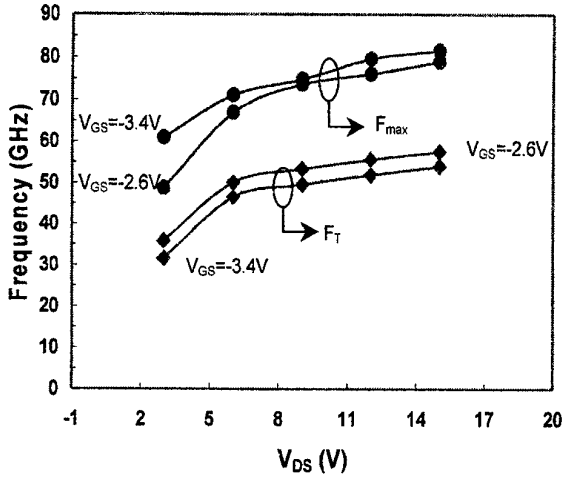


**Fig. 1** AlGaN/GaN MODFETs $f_{max}$ and $f_T$ under various bias conditions

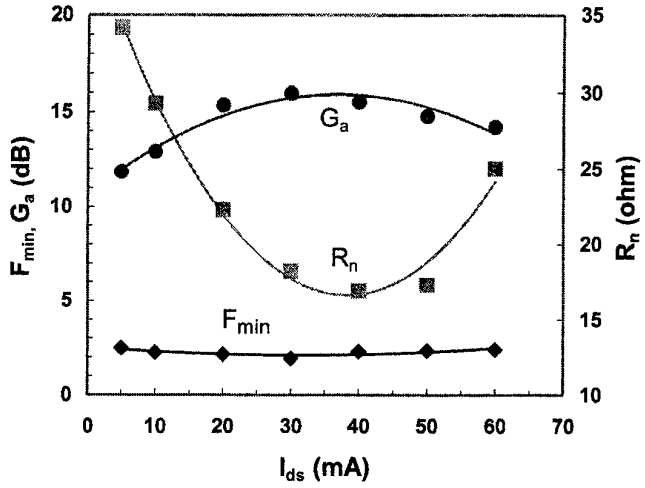


**Fig. 2** $F_{min}$, $G_a$ and $R_n$ as a function of drain current

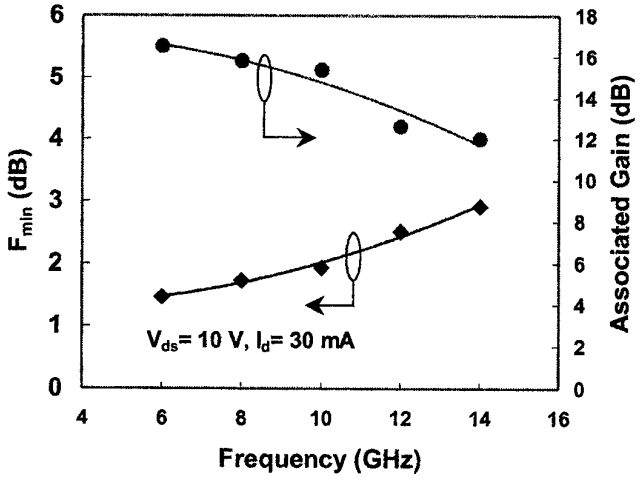


**Fig. 3** $F_{min}$ and $G_a$ as a function of frequency

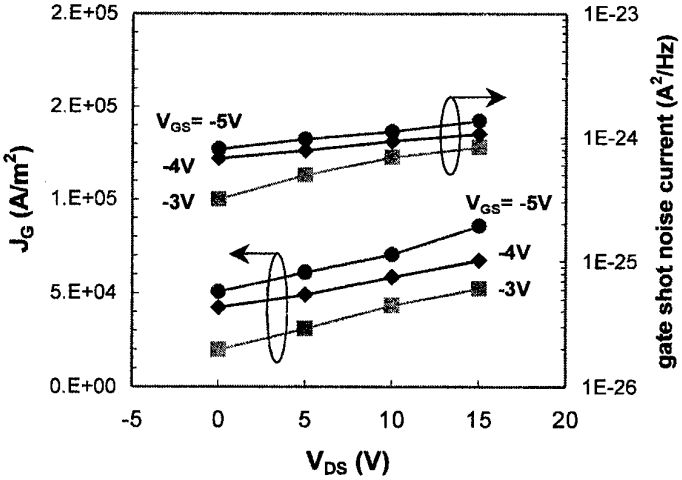


**Fig. 4** Gate leakage current density and corresponding shot noise current as a function of $V_{DS}$ and $V_{GS}$


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# Optimization of AlGaN/GaN HEMT structures using the RoundHEMT technology

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The electrical characterization of epitaxially grown HEMT layer structures for device fabrication is commonly performed by Hall measurements. However, the ultimate characterization of a HEMT layer system is the transistor device itself. The RoundHEMT concept [1] meets the need for a device technology with only a few fabrication steps that allows a fast feedback to epitaxy while allowing evaluation of important electrical and also processing data (Ohmic and Schottky contact, d.c. and pulsed output characteristics, optoelectronic properties, etc.). This device concept uses a gate formed as a closed ring, with the drain contact placed inside the gate ring. The source metallization encloses the gate completely, eliminating the need of mesa etching (Fig. 1). Because of its very simple and fast technology the RoundHEMT concept presents itself as an additional standard characterization tool for HEMT layer systems.

In this work we investigated the influence of the AlGaN barrier layer thickness and doping distribution on the electrical properties of modulation doped AlGaN/GaN HEMTs. To this end the AlGaN cap layer and doping layer thickness were varied as well as the latters doping height as shown in table 1, whereas the Al content and the separation layer thickness were kept constant at 18% and 5 nm, respectively. The structures were deposited on a 2.5 µm thick GaN buffer layer by MOVPE (AIXTRON) using conventional source materials and 2 inch c-plane sapphire substrates. Hall effect studies show a comparable conductivity for all the samples nearly independent of the sample structure. This suggests that the device characteristics could also be similar for all the samples. Using the RoundHEMT concept, however, the difference in electrical characteristics becomes unambiguously visible (Fig. 2). Here clearly sample B has superior characteristics to the other samples. This structure was then processed in conventional r.f. compatible HEMT technology. The HEMT showed state of the art high frequency data, i.e. $I_{DSS}$ = 700 mA/mm, $f_T$ = 35 GHz, $f_{max}$ = 70 GHz for $L_G$ = 200 nm (Figs. 3, 4). These results demonstrate the questionability of Hall effect investigations for evaluation of HEMT structures and the suitability of the RoundHEMT concept for structural optimization.

[1]: M. Marso, K. Schimpf, A. Fox, A. v.d.Hart, H. Hardtdegen, M. Hollfelder, P. Kordoš, and H. Lüth, Novel HEMT layout: The RoundHEMT, Electronics Letters **31**, 589 (1995)

Table 1: Important parameters of the investigated layer systems

| Sample | A | B | C | D |
|---|---|---|---|---|
| ***layer structure*** | | | | |
| cap layer thickness [nm] | 6 | 12 | 12 | 12 |
| carrier supply layer thickness [nm] | 10 | 10 | 10 | 15 |
| carrier supply layer doping [$cm^{-3}$] | 5E18 | 5E18 | 2E18 | 2E18 |
| ***Hall effect results*** | | | | |
| Hall sheet concentration [$cm^{-2}$] @ 300K | 4.7E12 | 5.75E12 | 5.46E12 | 5.78E12 |
| Hall sheet concentration [$cm^{-2}$] @ 77K | 5.66E12 | 5.97E12 | 5.46E12 | 5.85E12 |
| Hall mobility [$cm^2/Vs$] @ 300K | 1335 | 1091 | 1119 | 1207 |
| Hall mobility [$cm^2/Vs$] @ 77K | 5894 | 3218 | 3247 | 5811 |
| ***RoundHEMT ($L_G$ = 700 nm)*** | | | | |
| $I_{DS\,(1V)}$ / [mA/mm] | 130 | 354 | 210 | 290 |
| gm,max [mS/mm] | 79 | 132 | 104 | 119 |

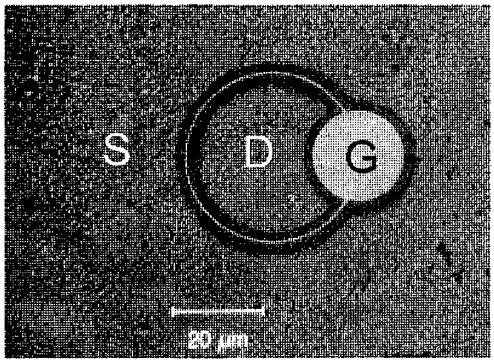


Fig. 1: Viewgraph of a RoundHEMT
channel width = 100 µm
S-D = 4 µm, $L_G$ = 700 nm

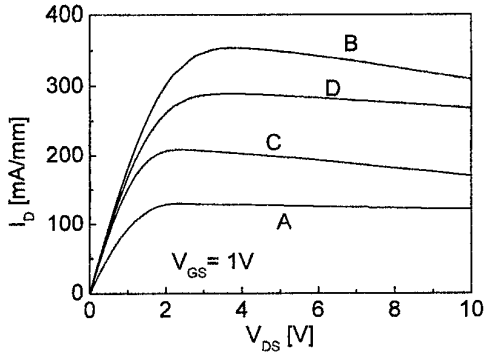


Fig. 2: Output characteristics of Round-HEMTs fabricated with the investigated layer systems
(S-D = 4 µm, $L_G$ = 700 nm)

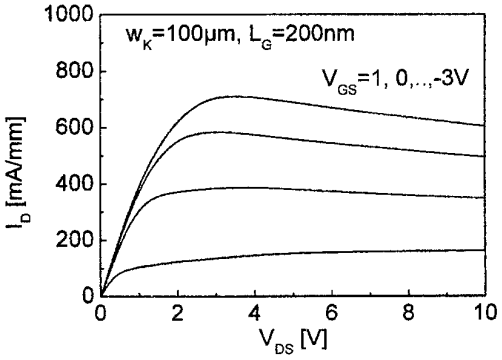


Fig. 3: Output characteristics of an r.f. optimized HEMT (sample B)
(S-D = 2 µm, $L_G$ = 200 nm)

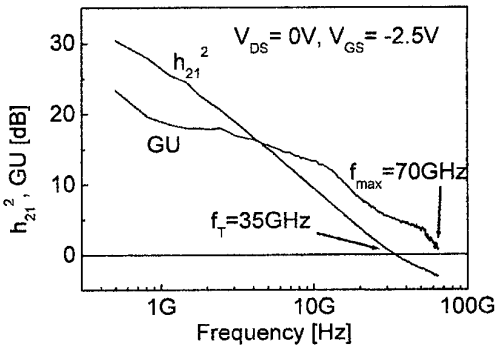


Fig. 4: r.f. behaviour of optimized HEMT(sample B)
(S-D = 2 µm, $L_G$ = 200 nm)

# Characterization of Temperature Dependence of AlGaN/GaN HEMTs

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GaN-based devices have received much attention for their ability to operate at high-power level and in high-temperature environment. In order to fully develop the potential of the device at high temperature, it is very important to evaluate the high temperature performance of the device not only at DC but also at high frequency. However, there are few reports which studied the high-frequency performance at high temperature [1][2]. In this report, we investigated the high-frequency performance of AlGaN/GaN HEMTs at temperatures up to 187 °C. The effective electron velocity in the channel was also evaluated.

Fig.1 shows schematic cross-section of the AlGaN/GaN HEMT fabricated on an epitaxial layer grown by MOCVD. The ohmic contacts were formed by evaporating Ti/Al (25/250 nm) and alloying at 650 °C for 30 s. 1.3-μm Schottky gate was formed by Ni/Au (12/250 nm) evaporation and the subsequent lift-off process.

The measurements were performed at temperatures between 23 and 187 °C in an air atmosphere. The I-V characteristics of the fabricated device at 23 and 187 °C are shown in Fig.2 by solid and open circles, respectively. The transconductance $g_m$ and the drain current $I_D$ were 110 mS/mm and 480 mA/mm at 23 °C, and 72 mS/mm and 320 mA/mm at 187 °C, respectively. They decreased gradually with increasing temperature. The decrease at high temperatures is probably due to the decrease in 2DEG mobility and electron velocity. Stable operation was confirmed even at 187 °C, suggesting the stability of the present ohmic and gate contacts.

Fig.3 shows the cutoff frequency $f_T$ as a function of $V_{DS}$ at $V_{GS}$ = −1.5V evaluated at various temperatures. The $f_T$ increased as the $V_{DS}$ increased, showed a peak at $V_{DS}$ about 10 V, then gradually decreased. The increase at small $V_{DS}$ is due to the increase of the electric field in the channel, and the decrease at large $V_{DS}$ is due to the extension of gate depletion region toward the drain electrode. The $f_T$ was decreased with increasing temperature. Fig.4 shows the $f_T$ as a function of $V_{GS}$ at $V_{DS}$ = 10 V. At 23 °C, the highest $f_T$ of 14 GHz was obtained at $V_{GS}$ = −1.5 V, and the $f_T \times$ gate-length product of 18 GHz·μm was among the highest achieved for GaN-channel FETs. Similar $V_{GS}$ dependence was obtained for different temperatures as shown in Fig.4.

Fig.5 shows the $f_T$ at $V_{DS}$ of 10 V and the $V_{GS}$ of −1.5 V as a function of temperature. The decrease in $f_T$ by increasing temperature from 23 to 187 °C was 35%. The $f_T$ decrease reflects the decrease of effective electron velocity in the channel.

In order to evaluate the effective electron velocity in the channel, the total delay time ($\tau = 1/2\pi f_T$) was plotted as a function of the inverse of $I_D$ at $V_{DS}$ = 10 V as shown in Fig.6 at various temperatures. The delay time decreased linearly with decreasing the inverse of $I_D$ at small $I_D$ regime. The extrapolated intersect at $1/I_D = 0$ corresponds to the transit time under the gate ($L_G/v_{eff}$), if the parasitic delay time was sufficiently small [3]. The effective electron velocities obtained here from the transit time are 1.2, 1.1, and $0.8\times10^7$ cm/s at 23, 103, and 187 °C, respectively. The temperature dependence of $v_{eff}$ was shown by open circles in Fig.5. The temperature dependence of the velocity is quite similar to that of $f_T$. This suggests that the temperature dependence of $f_T$ is dominated by that of $v_{eff}$.

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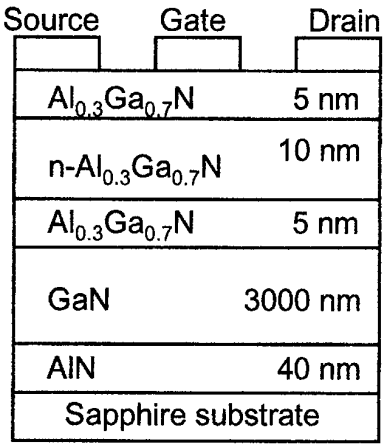


Fig.1 Schematic cross-section of the fabricated AnGaN/GaN HEMTs.

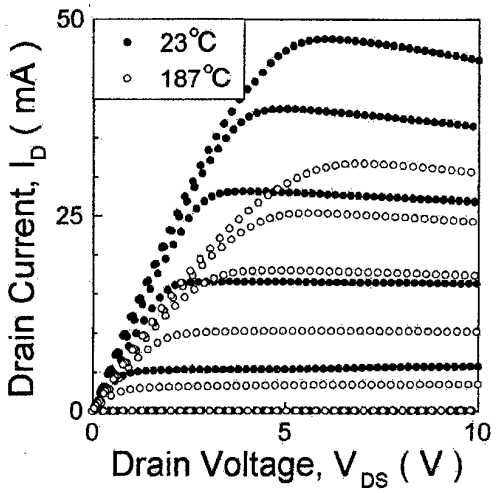


Fig.2 I-V characteristics at 23 and 187 °C; $V_{GS}$ = +1 ~ –4V. Gate width is 100μm.

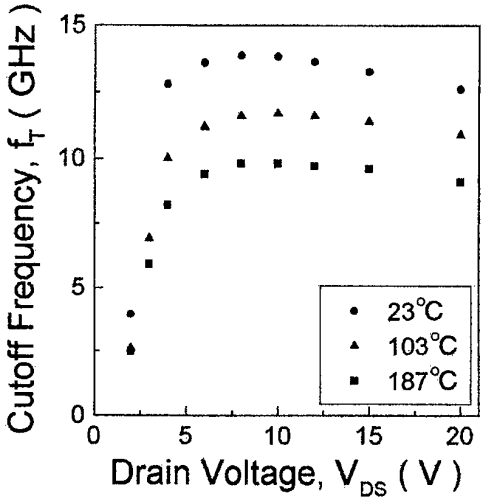


Fig.3 Cutoff frequency as a function of $V_{DS}$ at $V_{GS}$ = -1.5 V.

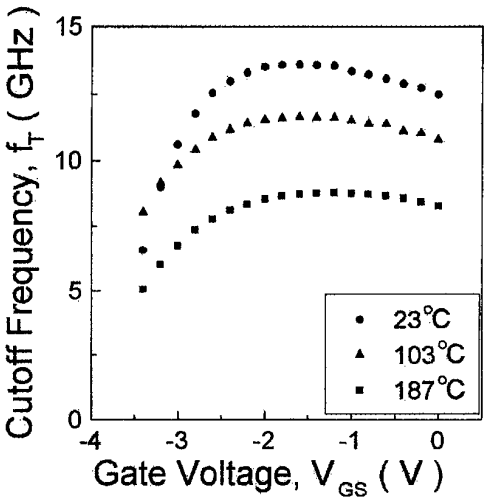


Fig.4 Cutoff frequency as a function of $V_{GS}$ at $V_{DS}$ = 10 V.

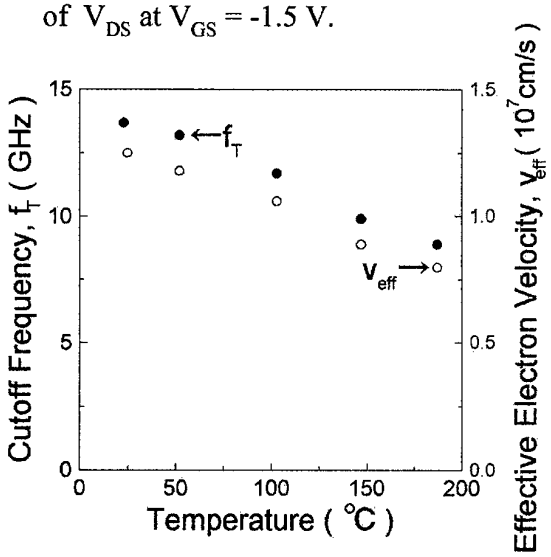


Fig.5 Temperature dependences of the cutoff frequency and effective electron velocity; $V_{DS}$ = 10 V, $V_{GS}$ = -1.5 V.

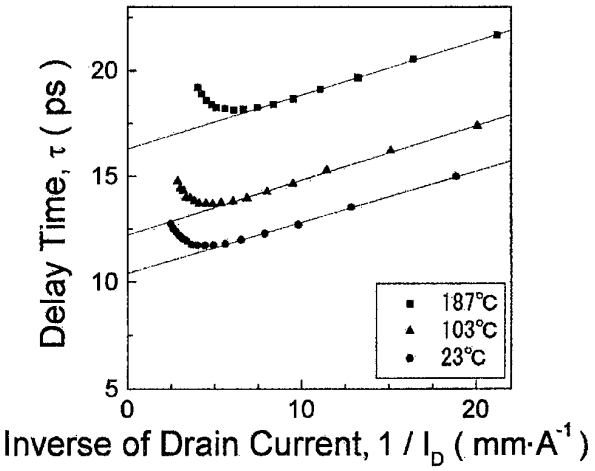


Fig.6 Delay time as a function of the inverse of $I_D$; $V_{DS}$ = 10 V.

# Influence of Barrier Thickness on the High Power Performance of AlGaN/GaN HEMTs

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HIGH power, high efficiency microwave transistors, amplifiers and switching devices are in demand for both commercial and defence applications. The inherent advantages of group III nitrides, like large band gap (3.4 eV), break down fields (> 2 MV/cm) and high electron velocities ($1.8 \times 10^7$ cm/s) make the material system ideally poised to cater to this demand. Record output powers of 9.8 W/mm at 8 GHz have been reported [1] on transistors fabricated on group III nitrides shows the potential of these material systems. A $f_t$ of 101 GHz has been measured for AlGaN/GaN HEMTs with 0.1 $\mu$m which opens up applications at mm wave frequencies also [2].

Many groups have shown that there exists a current slump or dispersion at RF frequencies in the AlGaN/GaN material system due to which the current available at RF is less than at DC [3]. This effect translates into the output power at microwave frequencies being less than what can be expected from the DC characteristics. Efforts have been underway to understand the effect in several laboratories [4], [5]. The current slump is attributed to acceptor like states arising from threading dislocations and surface states near the gate [4]. These states trap electrons which are field emitted from the gate and cause the depletion of the two dimensional electron gas (2DEG). These electrons cannot contribute to the RF swing as they have lifetimes in the millisecond range [6] This reduces the current at RF and is detrimental to the large signal performance of the device. In this paper we show that the effect is increased if the barrier thickness is decreased. Figure 1 shows the RF load lines plotted against the IV curves on $2 \times 125 \times 0.3\mu$m AlGaN/GaN HEMT made on SiC substrates with AlGaN thicknesses of 10nm and 20nm. The HEMT made on a 10nm barrier gave a saturated output power of 1.2 W/mm at 8 GHz whereas the 20nm barrier gave a saturated output power of 2.65 W/mm at 8 GHz. Both the devices were biased at $V_D = 25$V and class A operation. Note that the DC operation of the 2 devices were very similar and cannot explain the discrepancy in the large signal performance. The RF full channel current measured for the 10nm barrier device is half that of the 20nm barrier device and the RF knee voltage measured for the 10nm barrier device is 19V as against the DC knee voltage of 5V and for the 20nm barrier device the RF knee voltage is 14V as against the DC knee voltage of 5V. These factors limit the performance of the 10nm barrier device as compared to the 20nm barrier device. This discrepancy can be explained by the increase in electric fields in the barrier which enhance the tunneling of electrons from the gate thereby increasing both the trapped charge and the depletion of the 2DEG. This effect can be mitigated if we apply a layer of silicon nitride on the device. The layer of silicon nitride prevents the trapping of electrons on the surface and so increases the PAE and the output power of these devices [8]. When a layer of silicon nitride was applied on devcies with a 20nm AlGaN barrier the performance improved dramatically. A $2 \times 100 \times 0.3\mu$m transistor gave a saturated output power of 8.8 W/mm (40% power added efficiency) at 10 GHz. This represents the state of the art performance of FETs for this periphery and frequency.Thermal dissipation becomes important once passivation is performed as heating of the devices significantly degrades the mobility [7]. This is especially true when operating at high drain biases for high power operation.

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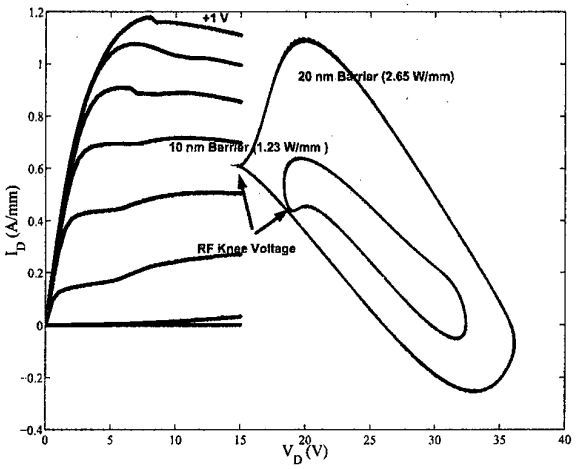


Fig. 1. Loadlines measured on $2 \times 125 \times 0.3\mu$m devices without passivation. Thin barrier device biased at $V_D = 25$V and $V_G = -1$V and the 20 nm barrier device biased at $V_D = 25$V and $V_G = -2.5$V. Note the RF knee voltage is significantly different from the DC knee voltage and the RF full channel current of the 10nm barrier is half that of the 20nm barrier device.

## ACKNOWLEDGMENTS

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# An investigation into the charge distribution and pinch off behavior of AlGaN/GaN double heterostructure DH-FETs under Schottky and ohmic contacts.

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We have fabricated AlGaN/GaN single heterojunction SH-FETs and $Al_xGa_{1-x}N/GaN/Al_yGa_{1-y}N/GaN$ double heterojunction DH-FETs and found that the DH-FETs can tolerate a higher gate bias before significant leakage occurs. Therefore we investigated the DH-FETs in a systematic way to understand the best compromise in current driving capability and control. A high 2DEG density in the GaN quantum well (QW) under an ohmic contact with low barrier height i.e. $\varphi_b$ <0.5eV and a depleted GaN QW for a schottky contact with $\varphi_b$ >1eV was aimed for. Heterostructures consisting of a 50Å $Al_{0.3}Ga_{0.7}N$/50Å $GaN/Al_yGa_{1-y}N$ were grown by radio frequency (RF)-molecular beam epitaxy (MBE) on $n^+$ GaN buffer layers on $Al_2O_3$. The AlGaN lower barrier width was varied between 100Å-1000Å and the composition from y=0.15 to y=0.3. Ni/Au schottky and Ti/Al ohmic contacts were deposited on different parts of the surface after making a circular mesa. No annealing was performed. The DHs were investigated by capacitance-voltage (CV) profiling in conjunction with self consistent Poisson-Schrödinger (SCPS) calculations of (i) the conduction band (CB) profile, two dimensional electron gas (2DEG) distribution and (ii) the variation of capacitance with applied gate bias $V_g$.

For the Schottky contacts we find one major peak in the concentration $N_{cv}$ vs depth curve in all DHs, located beyond the QW, based on the 'classical' analysis for a uniform layer under depletion. This is due to the gradual depletion of the single sub-band that exists below the fermi-level (FL) in the quasi-triangular potential well beyond the GaN QW. Its density drops linearly with applied gate bias $V_g$ giving a capacitance dQ/dV that is initially constant . The GaN QW has a negligible 2DEG density so it has no effect on dQ/dV during the depletion process. For the DH with $t_{LB}$=200 Å and y=0.2 there is a single sub-band below the FL at the AlGaN/GaN heterojunction, with a density of $7.8x10^{12}cm^{-2}$ at equilibrium and gives a calculated dQ/dV=17pF in good agreement with the measured value of 18pF. At the onset of pinch off, once the ground sub-band is over the FL, dQ/dV drops until there are no more confined states, after which the depletion edge starts moving into the GaN buffer. We find a strong dependence of pinch-off voltage $V_p$ on the lower barrier width e.g for $t_{LB}$=200 Å , $V_p$ =3V increasing to 5V for 400 Å and 16V at 1000 Å in good agreement with theoretical values. In contrast to the

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rectifying IV curves obtained with Ni/Au schottky contacts we found linear IV behavior for the Ti/Al contacts as deposited i.e. with no annealing. This is attributed to resonant tunneling through the double barriers as shown by calculations of the transmission coefficient by the transfer matrix method employing airy functions [2].

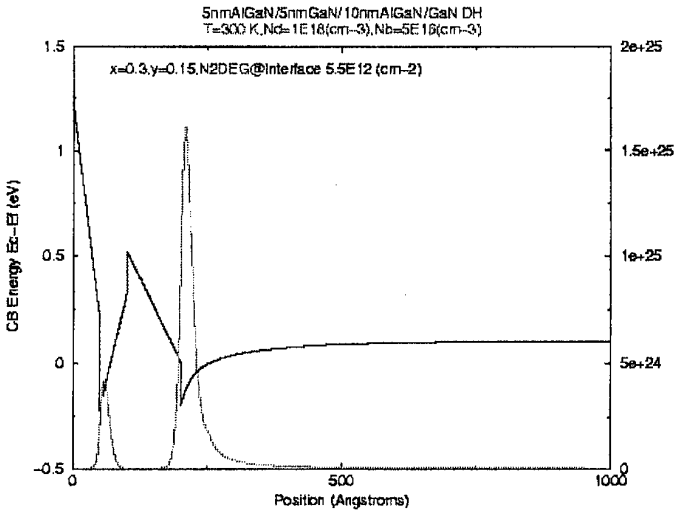


Fig 1. Conduction band *profile* of a 5nmAlGaN/5nmGaN/10nmAlGaN DH-FET showing the 2DEG distribution which has a sheet density of $5.5 \times 10^{12}$ $cm^{-2}$.

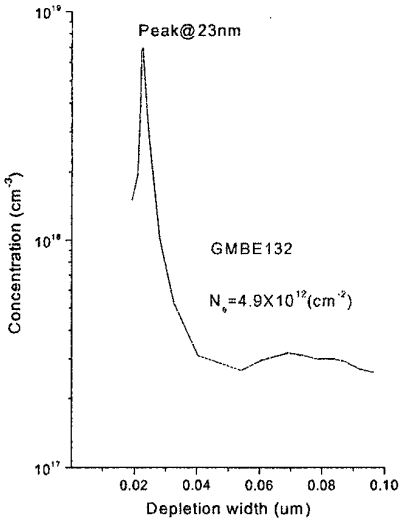


Figure 2. Capacitance-voltage profile of the same DH-FET in Fig 1. The integrated, sheet density is $4.9 \times 10^{12}$ $cm^{-2}$ in good agreement with the theoretical value.

[2] *We acknowledge support from the GSRT PENED 99ED 320 and bilateral cooperation projects.*

# SESSION XI
# SiC- and GaN-based devices
# Chair: Prof. Fausto Fantini
# Wednesday May 30, 2001

| | |
|---|---|
| **10.40 am**<br><br>**INVITED** | **Wide Bandgap Semiconductors Technologies for Microwave Power Amplifiers**<br>*C. Brylinski*<br>THALES LCR (formerly Thomson-CSF/LCR) Domaine de Corbeville, F-91404 Orsay Cedex |
| **11.05 am** | **Optimisation of Structure and Gate Leakage Effects in MOVPE AlGaN/GaN Heterostructure Field Effect Transistors**<br>*W S Tan[a], P A Houston[a], P J Parbrook[a], D A Wood[a], G Hill[a], C R Whitehouse[a] R W Martin[b]*<br>(a) Department of Electronic and Electrical Engineering, University of Sheffield, Mappin Street, Sheffield S1 3JD, UK.<br>(b) Department of Physics, University of Strathclyde, Glasgow, UK. |
| **11.20 am** | **ECR-Silicon nitride passivation of III-V transistor**<br>*S.Shapoval[a], V.Gurtovoi[a], A.Kovalchuk[a], and C.Gaquiere[b]*<br>(a) Institute of Microelectronics Technology, Russian Academy of Sciences, 142432 Chernogolovka, Moscow district, Russia.<br>(b) Institut d'Electronique et de Microelectronique du Nord, 9929 Dep. Hyperf. et Semic. Avenue Poincare B.P. 69 59652 Villeneuve D'ascq Cedex - FRANCE |
| **11.35 am** | **The Optoelectronic Response of Extended Defects in 4H-SiC**<br>*Chi-Hsin Chiu[a], P J M Parmiter[b], K Hilton[b], M J Uren[b] and J G Swanson[a]*<br>(a) Department of Electronic Engineering, King's College London, Strand, London, WC2R 2LS, United Kingdom<br>(b) DERA MALVERN, St Andrews Rd, Malvern, Worcs, WR14 3PS, United Kingdom |
| **11.50 am** | **4H-SiC p+-n-n+ Zener and IMPATT diodes**<br>*K. Vassilevski[a,b], K. Zekentes[a,b], M. Lagadas[a], N. Papanicolaou[c], A. Zorenko[d], Leonid Romano[e]*<br>(a) Foundation for Research and Technology-Hellas, P.O. Box 1527, Vassilika Vouton, 711 10 Heraklion, Greece<br>(b) Ioffe Institute, St.Petersburg, 194021,Russian Federation<br>(c) Naval Research Laboratory, 4555 Overlook Ave., Washington D.C. 20375, USA<br>(d) State Scientific & Research Institute "Orion", Kyiv, 252057, Ukraine<br>(e) "Svetlana-Electronpribor" Co., St. Petersburg, 194021, Russian /federation |
| **12.05 am** | **Trap-Related Effects in 6H-SiC Buried-Gate JFET's**<br>*G. Meneghesso[a], A. Chini[a], E. Zanoni[a], G. Verzellesi[b], E. Tediosi[b], C. Canali[b], A. Cavallini[c], A. Castaldini[c]*<br>(a) Dipartimento di Elettronica e Informatica and INFM, Universita' di Padova, via Gradenigo 6/A, 35131 Padova, Italy<br>(b) Dipartimento di Scienze dell'Ingegneria and INFM, Universita' di Modena e Reggio Emilia, via Vignolese 905, 41100 Modena, Italy<br>(c) Dipartimento di Fisica and INFM, Universita' di Bologna, via. B. Pichat, 40100 Bologna, Italy |

# WIDE BANDGAP SEMICONDUCTORS TECHNOLOGIES FOR MICROWAVE POWER AMPLIFIERS

DR. Christian Brylinski

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# Optimisation of Structure and Gate Leakage Effects in MOVPE AlGaN/GaN Heterostructure Field Effect Transistors

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*Department of Electronic and Electrical Engineering, University of Sheffield, Mappin Street, Sheffield S1 3JD, UK.*

R W Martin
*Department of Physics, University of Strathclyde, Glasgow, UK.*

The transport characterisitics of the two-dimensional electron gas in AlGaN/GaN HFET structures have been measured as a function of AlGaN barrier thickness and composition using Shubnikov de Haas and Hall. The devices were fabricated on wafers grown by MOVPE with an AlGaN barrier of different thickness and Al composition. All layers were nominally undoped and gate lengths between 1-2 μm were used. For and 15nm barrier thickness (30%Al), Hall measurements at 300K and 4.2K indicate an $n_s$ value of $1.1 \times 10^{13}$ $cm^{-2}$ and $7.1 \times 10^{12}$ $cm^{-2}$, and μ of 1720 $cm^2V^{-1}s^{-1}$ and 13500 $cm^2V^{-1}s^{-1}$ respectively (Fig. 1). To date, this is one of the highest 2DEG mobilities for this sheet concentration ever achieved on AlGaN/GaN structures grown on sapphire substrates. However, exceeding the critical thickness drastically reduces both the 2DEG density and mobility as expected. The difference in $n_s$ values at the two temperatures is due to carrier freeze-out of conduction paths parallel to the 2DEG. Maximum transconductances of 180 mS/mm for a 0.9 μm gate were achieved.

Below pinch-off, gate leakage currents are due to electron tunnelling through the barrier, which rises exponentially with gate voltage and drain voltage (at constant gate voltage) and can be simply explained by the reduction in barrier thickness with gate reverse bias. Above pinch-off, the gate leakage current rises much less rapidly with both gate and drain voltage, signifying the onset of the lateral expansion of the gate depletion region. These effects can be clearly seen from Fig.2. For devices with poor channel isolation (high buffer leakage) the gate leakage current is increased due to the higher vertical component of the field possible because of the lack of pinch-off. The gate leakage current, beyond pinch-off, increases with gate–source reverse bias due to the lateral spread of the field to fill the whole region under the gate.

Investigations of the gate leakage current with temperature show that the vertical leakage (gate at or below pinch-off) increases with temperature at a faster rate than the lateral leakage (Fig. 3). The reasons for this are unclear. However, the gate-drain breakdown voltage (~80 V at 20°C) reduces with increasing temperature, indicating that a breakdown mechanism other than impact ionisation may be responsible.

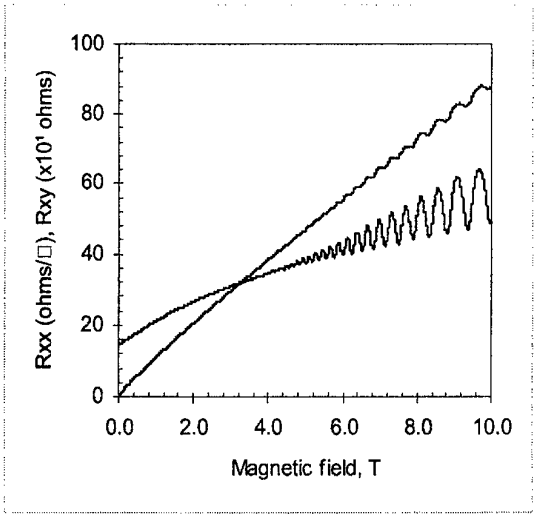


Fig. 1. Magnetoresistance (Rxx) and quantum Hall resistance (Rxy) for the 15nm barrier and 30% Al mol fraction structure at 4.2K, which yielded a record mobility of 13500 $cm^2V^{-1}s^{-1}$.

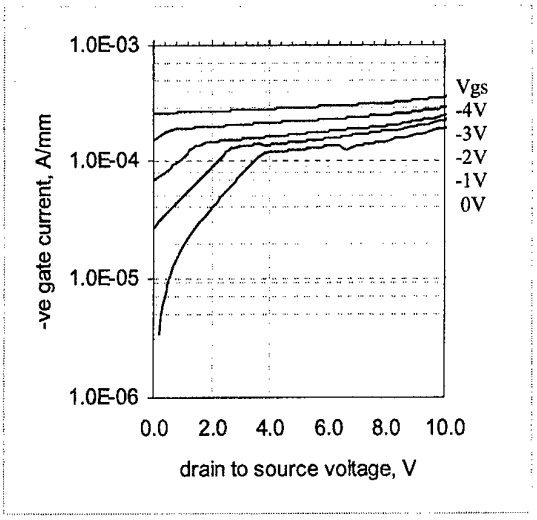


Fig. 2. Three-terminal gate leakage current vs drain-source voltage as a function of gate voltage. The gate pinch-off voltage is –4V. The transition from vertical to lateral leakage is evident for negative gate voltages less than 4V.

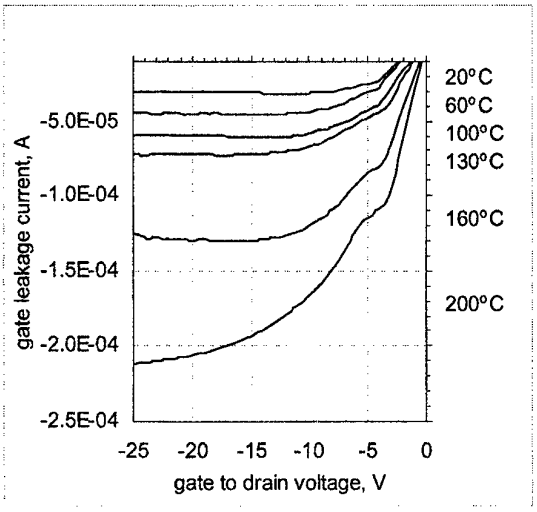


Fig. 3. Two-terminal gate-drain leakage current as a function of temperature.

# ECR-silicon nitride passivation of III-V transistors

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**Abstract.** We have studied the hydrogen incorporation in ECR silicon nitride films and their passivation effects for GaAs and GaN transistors. Silicon nitride films were deposited by varying substrate temperature (20-300°C), $SiH_4/N_2$ flow ratio (0.75-1.2), pressure (1-6 mTorr), and microwave power (200-500 W). Optical properties and H-content of the films were characterized by ellipsometry and Fourier transform infrared (FTIR) spectroscopy, respectively. Composition homogeneity of the films was determined by secondary ion mass spectroscopy and Auger electron spectroscopy. After passivation by hydrogen content optimized silicon nitride films, there were observed improvement in breakdown voltage for GaAs MESFETs and increase in saturation current for GaN HFETs.

Plasma-enhanced chemical vapor deposition (PECVD) of $Si_3N_4$ is widely used technique for device passivation and encapsulation in III/V technology. Due to advantages of electron cyclotron resonance (ECR) plasma methods with high plasma density ($10^{12}$ $cm^{-3}$) and low ion energy (~ 20 eV), they became very efficient tools for deposition and etching. Moreover, ECR $Si_3N_4$ gives high quality films with improved step coverage [1,2]. But contrary to PECVD, ECR CVD of $Si_3N_4$ is not so extensively studied. It has been reported that the trap densities increases with hydrogen concentration in silicon nitrides [3]. FET performance is also subjected to influence of hydrogen content in $Si_3N_4$ films [4].

In this work we have studied the hydrogen incorporation as a function of deposition parameters. The amount of hydrogen bonds in $Si_3N_4$ films influences both physical and electrical properties. Depending on bonding configuration (Si-H or N-H), hydrogen can increase the wet etching rate, change electrical properties, increase the residual stress, decrease the thermal stability. N-H bonds are responsible for the compressive stress of the $Si_3N_4$ film [5]. As for interface state density of $Si_3N_4$ on n-GaN, this system has been studied recently for PECVD $Si_3N_4$ [6].

Silicon nitride films (100-200 nm) were deposited from monosilane ($SiH_4$) and nitrogen diluted in argon (1:3) using an ECR plasma reactor. Silicon nitride films were deposited by varying substrate temperature (20-300°C), $SiH_4/N_2$ flow ratio (0.75-1.2), pressure (1-6 mTorr), and microwave power (200-500 W). To investigate $Si_3N_4$ film properties, the films were deposited on Si (100) wafers (p-type, 10 Ωcm). Silicon nitride refractive index in the range 1.96-2.03 was measured by varying the $SiH_4/N_2$ flow rate ratio (0.9-1.1). Figure 1 shows the normalized FTIR spectrum of a typical silicon nitride film. The amount of hydrogen incorporation and bonding configuration was determined from the absorbance of the Si-H and N-H stretch modes at 2180 and 3340 $cm^{-1}$, respectively. Hydrogen content in $Si_3N_4$ films as a function of $SiH_4/N_2$ flow rate ratio is shown in Fig. 2. For both Si-H and N-H bond content, sharp changes were observed with small deviations of $SiH_4/N_2$ around 1. The total hydrogen incorporation remained nearly constant.

Figure 3 shows Auger depth profiles of a $Si_3N_4$ film on Si. One can see that, the film is homogeneous and has oxygen free interface. The oxygen content is lower than 0.5 %, which is determined by detection limit of Auger spectrometer.

From high frequency C-V measurements, interface-trap density level was determined to be rather low $(0.5\text{-}2)\times10^{11}$ $cm^{-2}eV^{-1}$, showing high quality of $Si_3N_4/Si$ interface without comprehensive cleaning procedures prior to deposition.

For passivation experiments, GaAs MESFETs were used with average breakdown voltage of 10 V. $Si_3N_4$ passivation of these transistors resulted in increase of breakdown voltage up to 19 V, with the

average breakdown voltage of around 15 V, the saturation current and transconductance being practically unchanged. Annealing in dry nitrogen at 250°C for 30 minutes resulted in slight increase of the breakdown voltage.

A significant current reduction or frequency-dependent slum deteriorates the RF power performance of AlGaN/GaN HEMTs. This effect is caused by trapping states at the surface of semiconductor between the gate and drain. Therefore, the usage of $Si_3N_4$ passivation layer could eliminate the surface effects limiting the RF current. Figure 4 shows an after passivation improvement of DC I-V characteristics for a GaN/AlGaN transistor with a gate of $2\times50\times0.3$ $\mu m^2$.

**References.**


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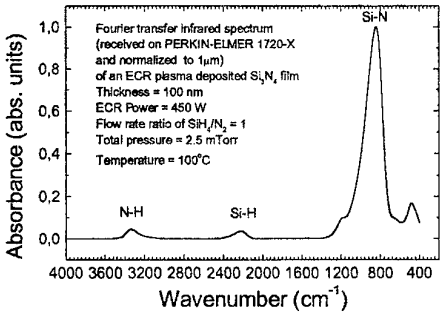


Fig. 1. FTIR spectrum of a $Si_3N_4$ film.

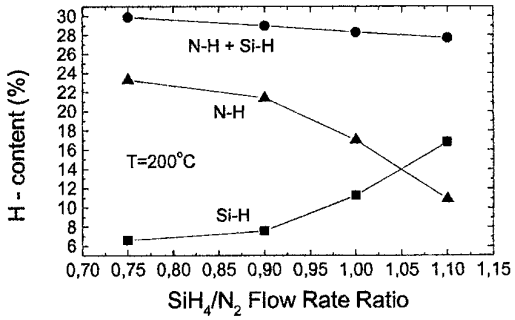


Fig. 2. Hydrogen content in $Si_3N_4$ films as a function of $SiH_4/N_2$ flow rate ratio.

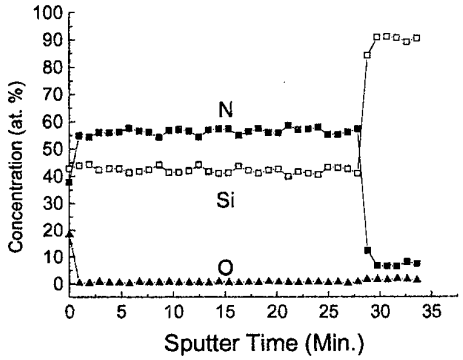


Fig. 3. Auger depth profile of an ECR plasma $Si_3N_4$ film deposited on Si

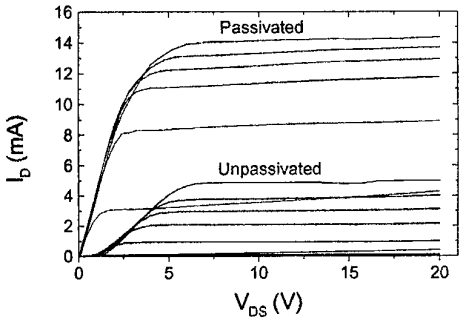


Fig. 4. DC I-V characteristics of GaN/AlGaN transistor (before and after passivation) with a gate of $2\times50\times0.3$ $\mu m^2$. Maximum $V_g$ =+4 V, step 1 V.

# The Optoelectronic Response of Extended Defects in 4H-SiC

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**United Kingdom**

Optoelectronic Modulation Spectroscopy(OEMS) senses the effect of light of definite photon energy on an electrical parameter associated with a semiconductor device structure. In this modulation spectroscopy the photon energy is periodically modulated and it is the modulation of the electrical parameter that is measured. The magnitude is then displayed as a spectrum as the mean photon energy is scanned. If the response is not in phase with the variation of photon energy the phase as well as magnitude can be plotted to form a pair of related spectra.

In this study OEMS was applied to a 4H-SiC MESFET in which channel conduction was determined by the thickness of the gate and backplane depletion regions, and by the carrier concentration and their average carrier mobility. If any of these parameters were affected by the incident light a change in channel current would be seen[1]. In this work sub band-gap photons were used to permit penetration into the semiconductor in order to excite charges in deep defect states. The table summarises the responses that were seen

The spectral feature at 1.2eV is of particular interest because it comprises two peaks separated by a phase change of 180°. It was the largest of the responses. Others were single peaked with a phase that indicated whether the response related to an electron or a hole trap. A model which takes into account the spread of the trap wavefunctions in k-space suggests that in this case the state was an electron trap, delocalised in real space with an extension of about 17nm, corresponding to a spatially extended crystal defect. The same model suggests that the other single peaked OEMS responses were from states that were spatially well localised, possibly from point defects. It is known that threading dislocations have high densities in SiC epitaxial materials, this suggests that these may be related to this peculiar OEMS feature.

The table includes published optical admittance spectroscopy[2,3] and DLOS[4] observations. The form of the 1.2eV DLOS signature is consistent and another DLOS feature at 0.96eV has a similar form but was not seen using OEMS.

| | | | PREVIOUS WORK | |
|---|---|---|---|---|
| | **Trap type** | **Comments** | **Optical admittance [2,3]** | **DLOS[4]** |
| **Energy (eV) (293K)** | | | **Energy(eV) (40K)** | **Energy(eV)** |
| 0.72 | E/H | superimposed similar responses | 0.72 | |
| 0.80 | E | | | |
| 0.82 | E | | | |
| 0.88 | E | | 0.87 | |
| 0.92 | E | | | 0.96 (peak) |
| 1.01 | H | | | |
| 1.12 | E | | 1.10(SI) | |
| 1.20(150K) | E | delocalised | 1.18 | 1.25(peak) |
| 1.60 | E | | 1.60(SI) | |
| 1.76 | E | | 1.73 | 1.5-2.0(broad threshold) |
| 2.00 | H | | | |
| 2.20 | H | | | |
| 2.3-2.9 | H | unresolved | | |

This result is of particular interest because of its possible relevance to GaN epitaxial materials which often contain dislocation densities as high as $10^8 cm^{-2}$. There is strong evidence that dislocations limit the carrier mobility in GaN and they are often represented in conduction models as extended lines of charge. Their role in optical processes is less clear. OEMS might provide a means for distinguishing their behaviour and the method is currently being applied to see if similar "delocalised" signatures exist in these materials.

**References**


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**Acknowledgement**


Technology Groups 7 and 9 of the UK MoD Corporate Research Programme provided partial support and C-H C was supported by King's College London Taiwan Scholarship.

# 4*H*-SiC $p^+$-$n$-$n^+$ Zener and IMPATT diodes

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[5]*"Svetlana-Electronpribor" Co., St. Petersburg, 194021, Russian /federation*

The advantage of silicon carbide (SiC) as a semiconductor for use in ultra high frequency (UHF) diodes is based on its fundamental properties: high breakdown field, excellent thermal conductivity, capability to operate at elevated temperature. Nevertheless, fabrication of UHF SiC diodes was not extensively addressed up to now, although outstanding results were obtained in the development of high power/low frequency rectifying diodes. This fact may be attributed to the lack of diodes combining a low series resistance and a low capacitance in the same structure necessary for a UHF diode operation. Last year, we have reported [1] the fabrication of 4*H*-SiC $p^+$-$n$-$n^+$ diodes with record differential resistivity ($5\times10^{-5}\Omega.cm^2$ at DC forward current density j>25 kA/cm$^2$) and low capacitance value (down to 0.7pF for 40μm diameter). This paper reports on the use and characterization of these diodes as Zener and IMPATT diodes.

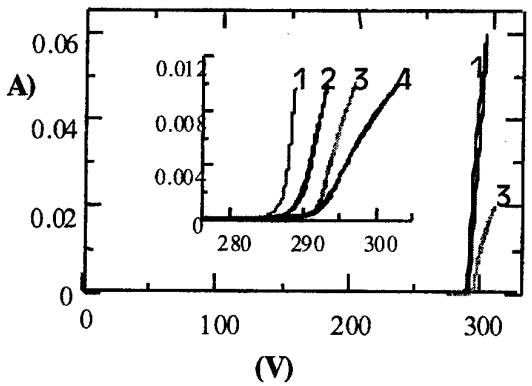


Fig 1. *I-V* characteristics of the 4*H*-SiC $p^+$-$n$ diode at maximum continuos avalanche current and at test current (shown in the insert) for various mesa structure diameters. 1 - diameter of mesa structure is 200 μm; 2 – 80 μm; 3 – 60 μm; 4 – 40 μm.

The diodes revealed stable operation at continuos avalanche current. Fig. 1 shows the *I-V* characteristics of 4*H*-SiC diodes having breakdown voltage about 290 V at maximum continuos current. Maximum continuos current of 60 mA was measured on the diodes with D=200 μm corresponding to the dissipated power of 18 W. The current was increased exponentially with applied voltage in the initial part of *I-V* characteristics until the diode self heating led to increasing of dynamic (or Zener) impedance $Z_Z$. It is clearly seen in the inset in Fig. 1. Parameters of the diodes depending on mesa structure diameter are given in the Table 1. The test current $I_{ZT}$, at which the Zener voltage ($V_Z$) and $Z_Z$ were measured, was chosen at minimum $Z_Z$ value. The scattering of $V_Z$ value through the wafer did not exceed 3%. All the diodes revealed the positive temperature coefficient (β) of $V_Z$ of about $3\cdot10^{-4}K^{-1}$ measured as at continuos current [2] as well as at high pulsed current conditions

To prove the advantage of SiC over silicon for fabrication of high voltage Zener diodes we have compared our diodes with commercial [3] Si Zener diodes with the same breakdown voltage. The SiC diodes with 200μm

| Mesa diameter or diode type | Capacitance at zero bias | Nominal Zener voltage at $I_{ZT}$ | Test current | Dynamic impedance $Z_Z$ (Ω) | | Maximum continuous current | Leakage current at $V_R$=230V | Typical temperature coefficient |
|---|---|---|---|---|---|---|---|---|
| D [μm] | $C_0$ [pF] | $V_Z$ [V] | $I_{ZT}$ [mA] | at 1mA | at $I_{ZT}$ | $I_{ZM}$ [mA] | $I_R$ [nA] | β [%/°C] |
| 40 | 0.7 | 295 - 304 | 3 | 1000 | 800 | 12 | 20 | 0.03 |
| 60 | 1.6 | 294 - 296 | 5 | 950 | 500 | 20 | 25 | 0.03 |
| 80 | 2.8 | 291 - 295 | 5 | 900 | 400 | 35 | 40 | 0.03 |
| 200 | 17 | 286-293 | 10 | 450 | 170 | 60 | 60 | 0.03 |
| 1N4993 | | 300 | 5 | 2100 | 800 | 15.6 | 2000 | 0.120 |
| 1N5110 | | 300 | 3 | | 1900 | 10 | 1000 | 0.105 |

Table 1. Parameters of 4*H*-SiC diodes with different mesa structure diameters and of commercial silicon Zener diodes[3].

mesa diameter were capable to operate at continuos current up to 60 mA corresponding to the power of 18 W. These diodes had dynamic resistance of 170 Ω at test current 10 mA, which is appreciably lower than that of Si diodes. At the same time they had lower leakage currents (about two orders of magnitude) and lower temperature coefficient of breakdown voltage.

The same diodes have produced ultra high frequency oscillations and thus the first 4H-SiC IMPATT diode has been demonstrated [4]. According to the theory of IMPATT oscillators, the fundamental frequency of free running IMPATT oscillator is lower than the transit time frequency, $f_T=v_S/2w_n$, and higher than the avalanche resonance frequency ($f_A$) of the diode. The value of $f_T$=19 GHz for fabricated 4*H*-SiC diodes may be easily calculated with use of $v_S=7.5\cdot10^6$cm/s, measured in [2]. To estimate the value of $f_A$, the noise power spectral density (NPSD) of fabricated diodes was measured [1]. Sharp decreasing of NPSD was observed at a frequency of about 6 GHz and this recession was moving to higher frequencies with increasing of $j_A$ and it was concluded that the value of $f_A$ must be higher than 6 GHz at operating current densities. The operating frequency of fabricated diodes was expected to be far from $f_T$ and close to $f_A$ due to the relatively high values of diode series resistivity ($R_S$). Taking into account that $f_A \sim \sqrt{j_A}$, the frequency range from 8.2 to 12.4 GHz (X-band) was chosen for microwave characterization of the diodes.

The maximum dc current density of 950A/cm$^2$ was passed through the diodes with mesa structure diameter of 40μm. This value of $j_A$ is much lower than anticipated operating current densities of SiC IMPATT diodes, therefore the pulsed mode of operation was chosen for microwave characterization. The diodes were biased with dc avalanche current of about 100nA to charge the capacitance of the *p-n* junction. Then, the current pulses having a width from 20 to 100ns were applied to the diode by a pulsed current source. The frequency of oscillations was measured by a cavity-resonator wavemeter, the average output power was measured by a thermistor microwave power meter. The microwave oscillations were detected by a microwave pulse detector connected through a directional coupler. The shape of input current pulse and the envelope of microwave pulse were measured by a two channel broad-band oscilloscope.

The microwave oscillations appeared at a threshold input pulse current of 0.3 A. The frequency of oscillations, of about 10 GHz, was located between the estimated values of $f_A$ and $f_T$. Fig. 2 shows a typical input current pulse (top trace) and a corresponding microwave video pulse (bottom trace) for one of the diodes. The transient thermal heating of the *p-n* junction led to the change of a diode impedance and, hence, of load matching conditions. This caused a chirp of the frequency through the pulse duration and a broad spectral distribution of the oscillations. This spectral broadening appeared as a noise on the top of the microwave video pulse, which is clearly seen in Fig. 2. Simultaneously, the frequency of oscillations measured at different moments during the pulse was varied from 9.9 to 11 GHz. A microwave pulsed power of about 300 mW was measured at the pulse current of 0.35 A and duration of 40 ns. The duty factor was 1:700. The power conversion efficiency was of about 0.3%. This relatively small efficiency can be explained by operating of the diodes at frequencies very close to $f_A$. It should be noted that further increasing of the output power was available, but this optimization was not performed. All the measurements were made near the threshold current to avoid the risk of a diode burnout.

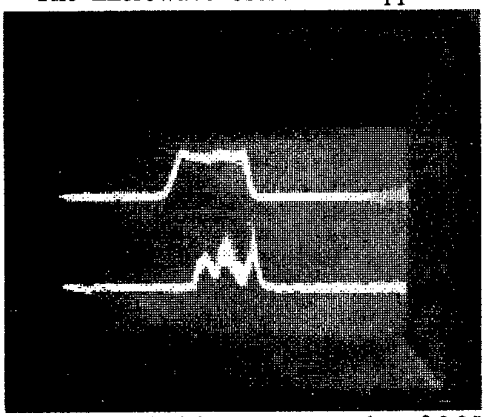

Fig. 2. A typical input current pulse of 0.35 A, 40 ns (top trace) and the corresponding output power video pulse (bottom trace) of the 4*H*-SiC IMPATT oscillator.

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# Trap-Related Effects in 6H-SiC Buried-Gate JFETs

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In this paper, deep levels are characterized in 6H-SiC, buried gate, n-channel JFETs by means of capacitance-mode (C-) and current-mode (I-) Deep Level Transient Spectroscopy (DLTS) and transconductance ($g_m$) frequency dispersion measurements. Moreover, the drain-current ($I_D$) transients following a gate-to-source voltage ($V_{GS}$) step are analyzed both experimentally and through two-dimensional device simulations allowing the different deep levels to be localized both energetically and spatially.

JFETs were fabricated by vacuum sublimation epitaxy on high-quality n-type, 6H-SiC platelets grown by an unmodified Lely process [1]. Figure 1 shows a schematic cross section of the JFET. The p-type, buried-gate layer is 5-$\mu$m thick and doped with Al to the concentration of $3\times10^{18}$ cm$^{-3}$. The n-type layer is doped with N to $3\times10^{17}$ cm$^{-3}$ and has a thickness $t_1 = 1.5$ $\mu$m, which is selectively reduced to $t_2 = 0.2$ $\mu$m to form the active channel region. The channel length and width are 8 $\mu$m and 760 $\mu$m, respectively. Typical electrical characteristics measured in these devices are [2]: threshold voltage, $V_P = -12V$, maximum saturated drain current, $I_{DSSmax}(V_{GS} = 0V) =$ 30 mA, maximum drain to source voltage, $V_{DSmax} = 100$ V.

C- and I-DLTS measurements revealed four distinct traps, having the following activation energies and apparent capture cross sections: $E_1 = 0.18$ eV, $\sigma_1 = 1.3 \times 10^{-16}$ cm$^2$; $E_2 = 0.19$ eV, $\sigma_2 = 1.0 \times 10^{-18}$ cm$^2$; $E_3 = 0.27$ eV, $\sigma_3 = 1.5 \times 10^{-18}$ cm$^2$; $E_4 = 0.59$ eV, $\sigma_4 = 1.2 \times 10^{-14}$ cm$^2$. Figure 2 shows the C-DLTS (left) and I-DLTS (right) spectra.

Figure 3 shows the normalized $g_m(f)/g_m(0.1\text{Hz})$ curve up to $f = 1$ MHz for temperatures ranging from -70 to +50 °C. Four slope changes can clearly be distinguished from Fig. 3; see arrows marked $E_1$, $E_2$, $E_3$ and $E_4$ for T = -70 °C. Slope changes occur in correspondence of characteristic frequencies which can be evaluated as the points at which the $\partial g_m/\partial f$ derivative peaks, $f_M$. From the temperature dependence of the characteristic frequencies, activation energies were extracted as the slopes of the Arrhenius plots shown in Fig. 4, which closely correlate to those provided by DLTS measurements.

Figure 5 shows the $I_D$ transients following a reverse-bias $V_{GS}$ step at different temperatures. At increasing temperature, the $I_D$ transient behavior is governed by increasingly deeper levels. Moreover, the different sign of the I-DLTS peaks shown in Fig. 2 (right) arises from the different dynamic behavior of the associated deep levels. Consistently, a "low-pass"-like response is observed at $T = 123$ K, which is in the temperature range where the negative I-DLTS peak associated with $E_1$ is located (see Fig. 2, right), while a "high-pass"-like response is obtained for $T = 223$ K, i.e. in correspondence of the positive I-DLTS peak related to $E_3$ (see Fig. 2, right). Finally, $E_4$ is most likely responsible for the "low-pass"-like behavior observed at $T = 323$ K, the latter falling in the temperature range of the associated C-DLTS peak (see Fig. 2, left). These results are also consistent with $g_m(f)$ measurements, in that traps $E_1$ and $E_4$ induce a downward (i.e. "low-pass"-like) dispersion, whereas $E_3$ is associated with an upward (i.e. "high-pass"-like) dispersion.

With the aim of correlating the JFET switching behavior to energetic and spatial location of traps, the following simulated experiments were carried out, using the drift-diffusion code DESSIS [3]. The $I_D$ response to a reverse-bias $V_{GS}$ step was simulated by assuming only one deep level among $E_1 \div E_4$ to be present within the device at a time. Each level was placed at its own activation energy either from the bottom of conduction band ($E_C$) or the top of valence band ($E_V$). In the first case, deep levels behave as electron traps, while, in the latter, they behave as hole traps. Moreover, each level was assumed to be either uniformly distributed in the n-channel or in the p-gate region. Temperature was set in all simulations to 300 K. Figure 6 shows normalized $I_D$ waveforms obtained when $E_3$ was considered. Similar $I_D$ curves (not shown) were also obtained for $E_1$, $E_2$, and $E_4$. As can be seen, dynamic effects are only observed when electron traps are put into the n-channel (see curve 1), or, dually, when hole traps are assumed to be present in the p-gate region (see curve 2). In the first case, a "high-pass"-like response is observed. In the latter, a "low-pass"-like response is instead obtained. Comparison of these results with measurements shown in Fig. 5 allows us to locate traps as follows: $E_3$ is an electron trap distributed in the n-channel region; $E_1$, $E_2$, and $E_4$ are hole traps located in the p-gate region.

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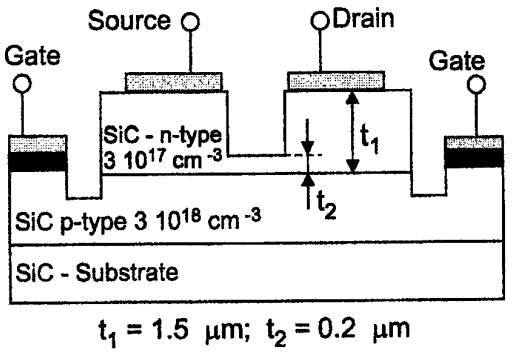


Figure 1: Schematic cross section of the buried-gate, n-channel JFETs

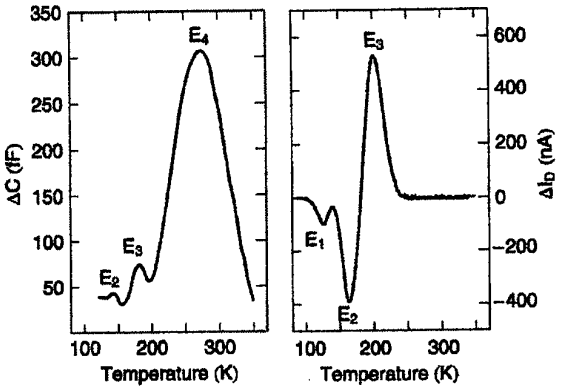


Figure 2: (a) Capacitance- (left) and current-mode (right) deep level transient spectroscopy spectra.

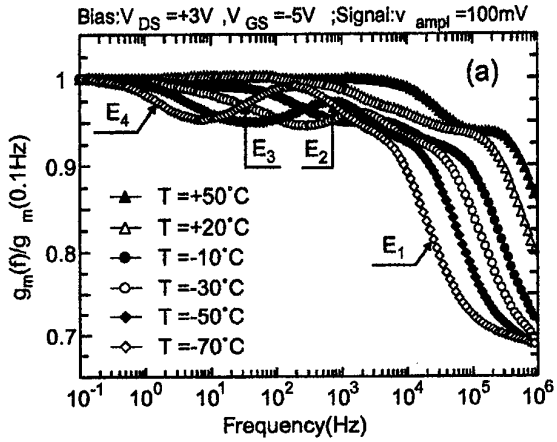


Figure 3: Normalized $g_m(f)/g_m(0.1\text{Hz})$ curves up to $f = 1$ MHz for temperatures ranging from -70 to +50 °C.

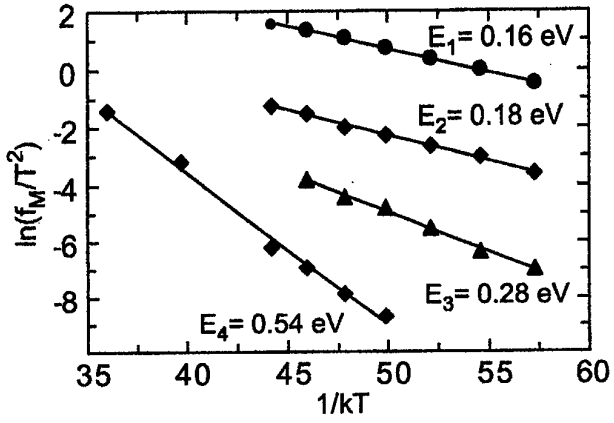


Figure 4: Arrhenius plot indicating the activation energies of the traps responsible for the $g_m(f)$ dispersion.

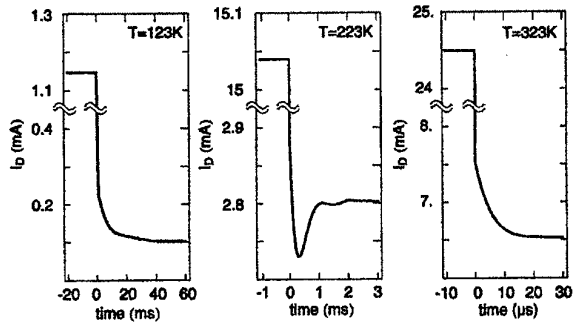


Figure 5: Experimental $I_D$ transients following a reverse-bias $V_{GS}$ step (from 0 to -6 V) at three different temperatures. The device was biased in the common-source configuration with an external resistance $R_D = 1$ kΩ connecting the drain to the power supply. The latter was adjusted to have $V_{DS} = 3$ V at $V_{GS} = -6$ V.

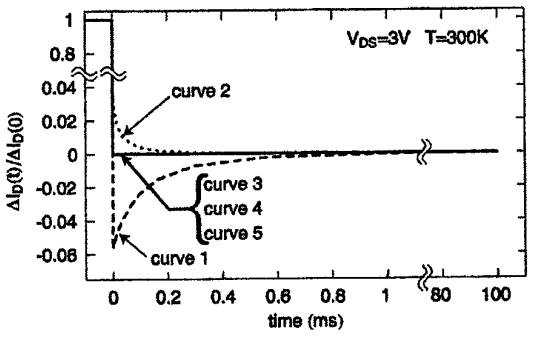


Figure 6: Simulated $I_D$ transients following a reverse-bias $V_{GS}$ step (from 0 to -1 V). Curve 1: $E_3$ at $E_C - 0.27$ eV and distributed in the n-channel. Curve 2: $E_3$ at $E_V + 0.27$ eV and distributed in the p-gate. Curve 3: $E_3$ at $E_C - 0.27$ eV and distributed in the p-gate. Curve 4: $E_3$ at $E_V + 0.27$ eV and distributed in the n-channel. Curve 5: no traps. $\Delta I_D(t)$ is defined as $\Delta I_D(t) = I_D(\infty) - I_D(t)$.

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